

Iris HSW/BDW Schematics

Broadwell-ULT

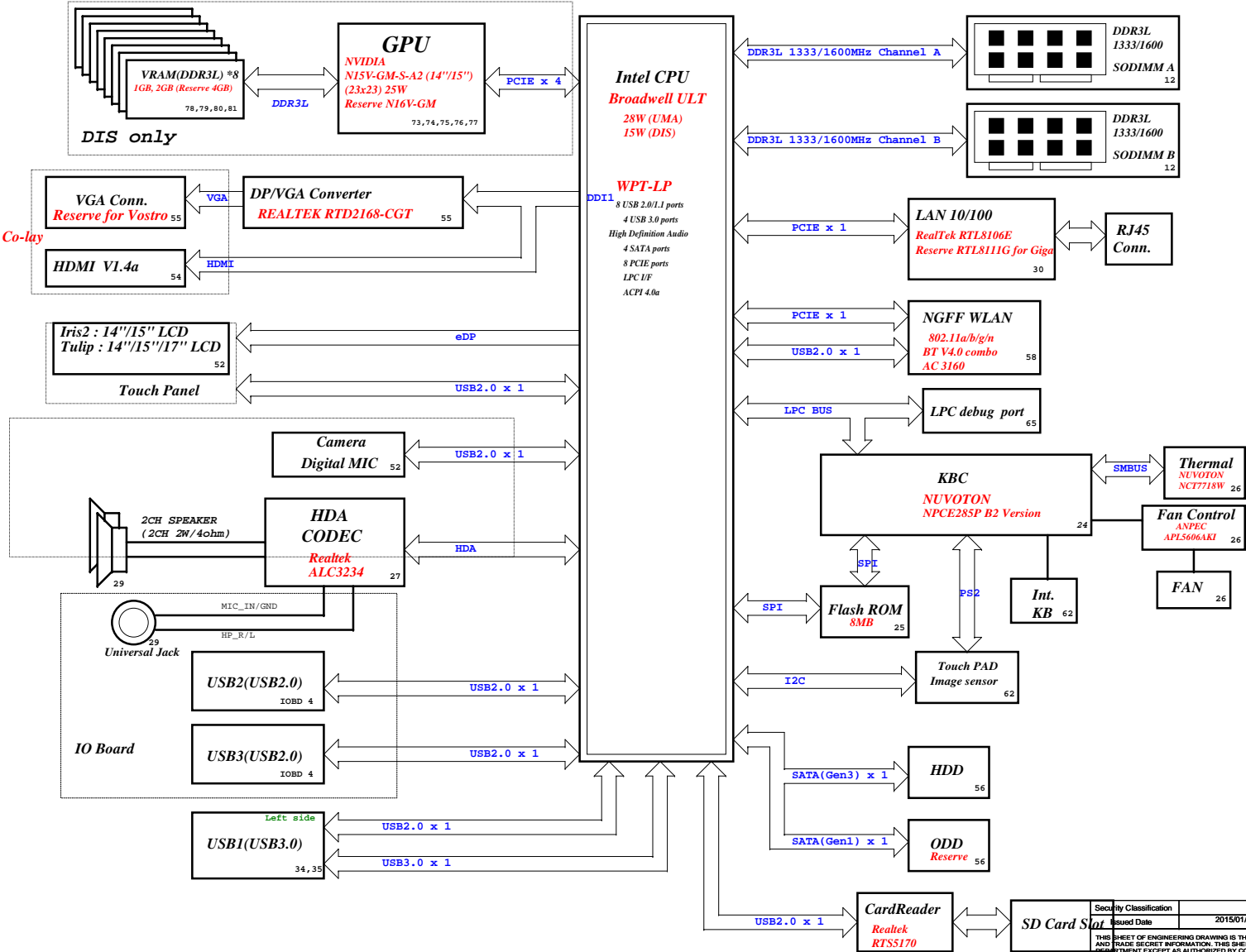
2015-01-20
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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					LA-B483P
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				Sheet	1 of 102
				Rev	A00

Project code:
Iris-2 14 --> 4PD031010001
Iris-2 15 --> 4PD032010001
PCB P/N: 14216
Revision: X01

Iris2/Tulip/VanGogh Block Diagram



CHARGER	
HFA0224RGRR-1-GP	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V AUX S5 5V AUX S5 5V S5 3D3V S5
CPU Core Power	
ISL95813HRZ-GP	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V S3 0D675V S0
CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V S0
CPU 1D5V_S0	
TLV70215DBVR-GP	51
INPUTS	OUTPUTS
3D3V S5	1D5V S0
Switches	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
PCB LAYER	
L1:Top	
L2:VCC	
L3:Signal	
L4:Signal	
L5:GND	
L6:Signal	

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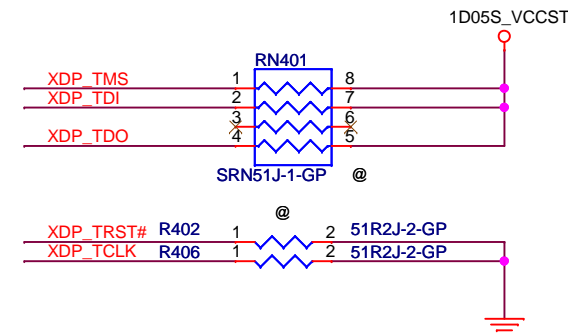
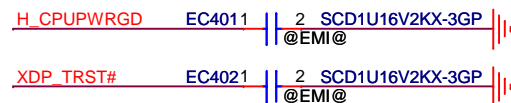
WWW.AliSaler.Com

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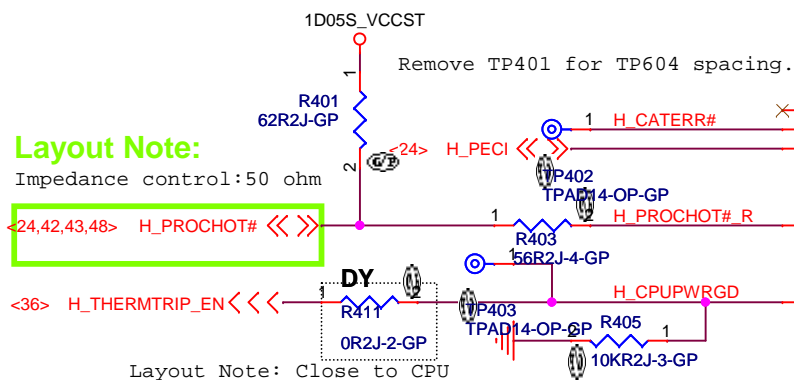
Main Func = CPU

For EMI Reserved

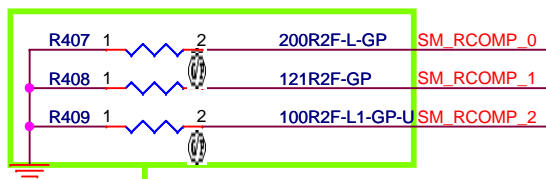


Layout Note:

Impedance control: 50 ohm



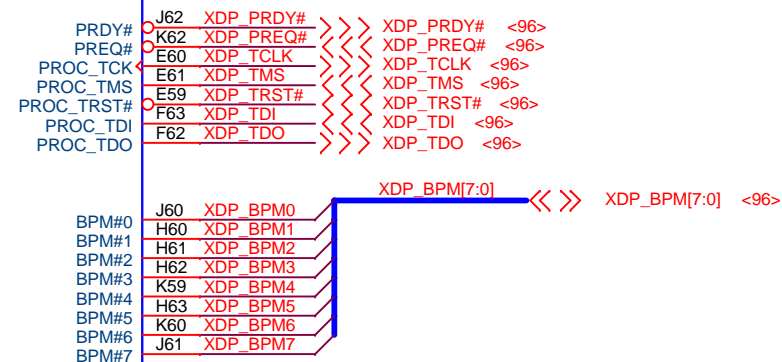
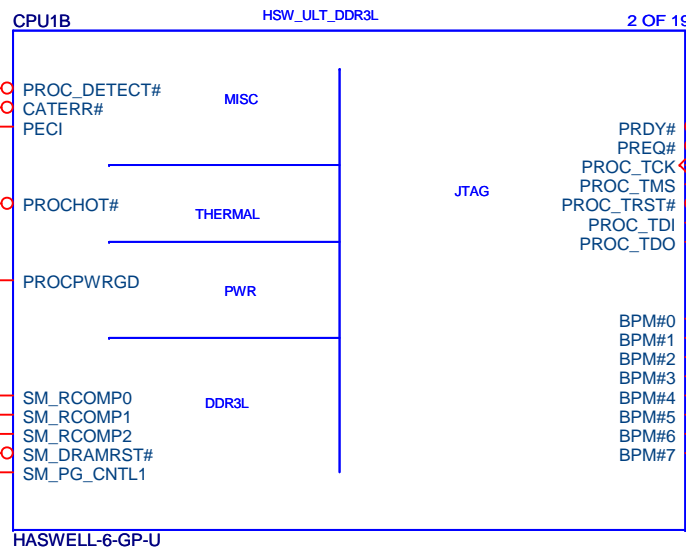
Layout Note: Close to CPU



Layout Note:

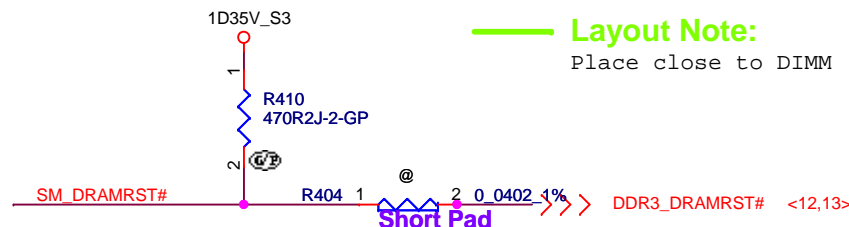
Design Guideline:

SM_RCOMP keep routing length less than 500 mils.



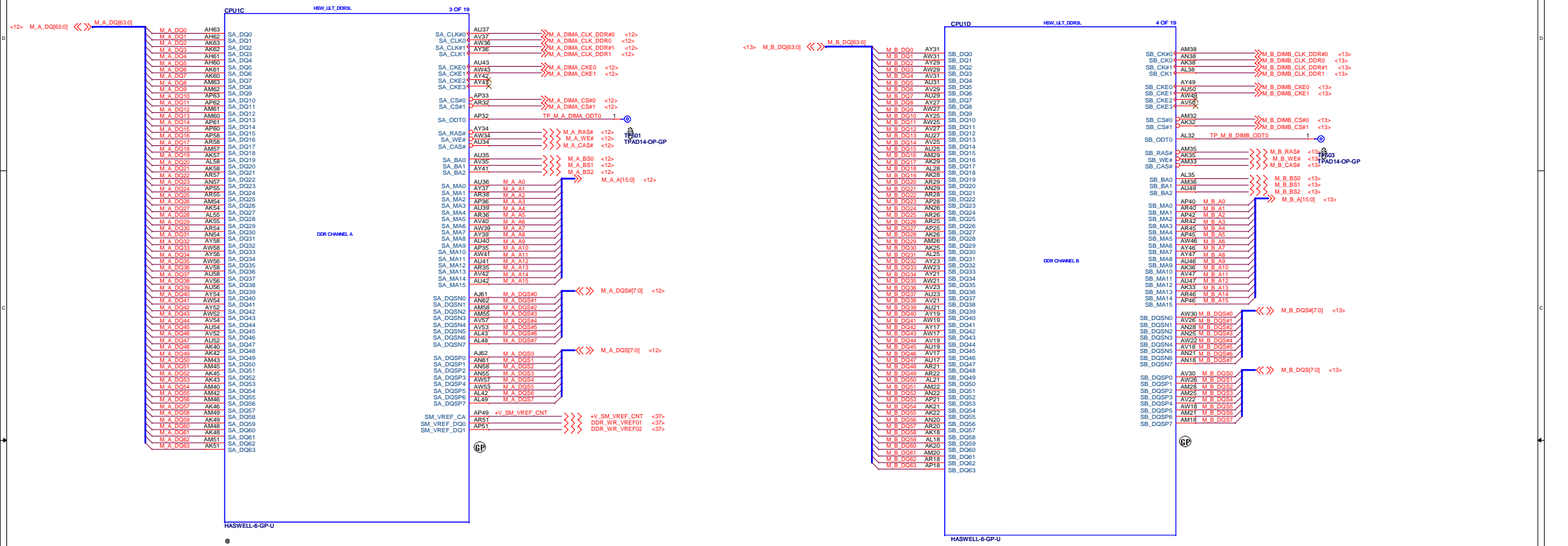
- **Layout Note:**

Place close to DIMM



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DDR3L ball type: Non-Interleaved Type



HSW

- CPU1 4030@
CL8064701552900 SR1EN D0 1.9G A31!
SA00007T1A1L
- CPU1 4005@
CL8064701478404 SR1EK D0 1.7G BGA
SA00007Z2QL
- CPU1 3205@
FH8065801882800 SR215 E0 1.5G FCBGA
SA000083H1L
- CPU1 5010@
FH8065801620406 SR23Z F0 2.1G FCBGA
SA00008982L
- CPU1 5200@
FH8065801620204 SR23Y F0 2.2G FCBGA
SA00008992L

Broadwell

- CPU1 BDW_PQ3@
FH8065801620003 QH15 E0 2.2G
SA000083A0L
- CPU1 3805@
FH8065801620702 SR210 E0 1.9G FCBGA
SA000083F2L
- CPU1 5005@
FH8065801884006 SR244 F0 2G FCBGA
SA000083E3L
- CPU1 5500@
FH8065801620004 SR23W F0 2.4G FCBGA
SA000089A2L

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D

C

B

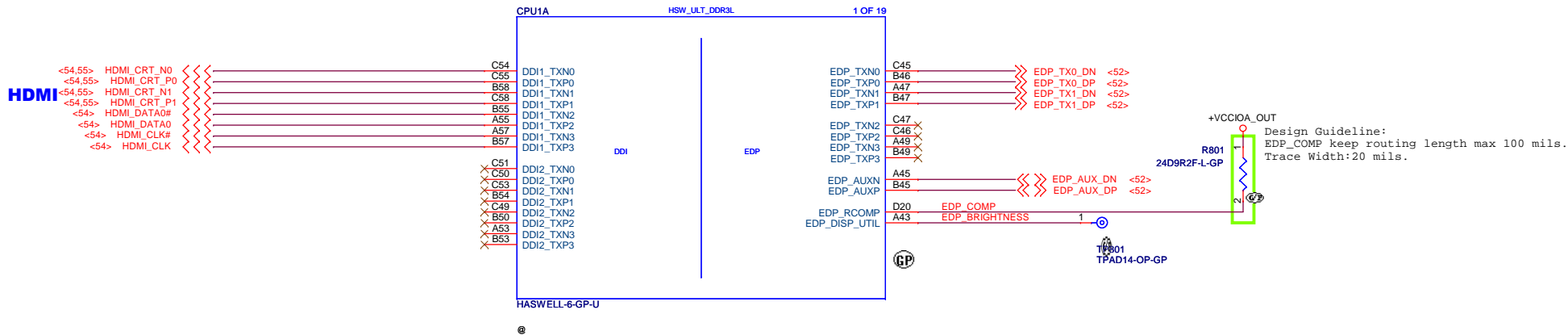
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D

C

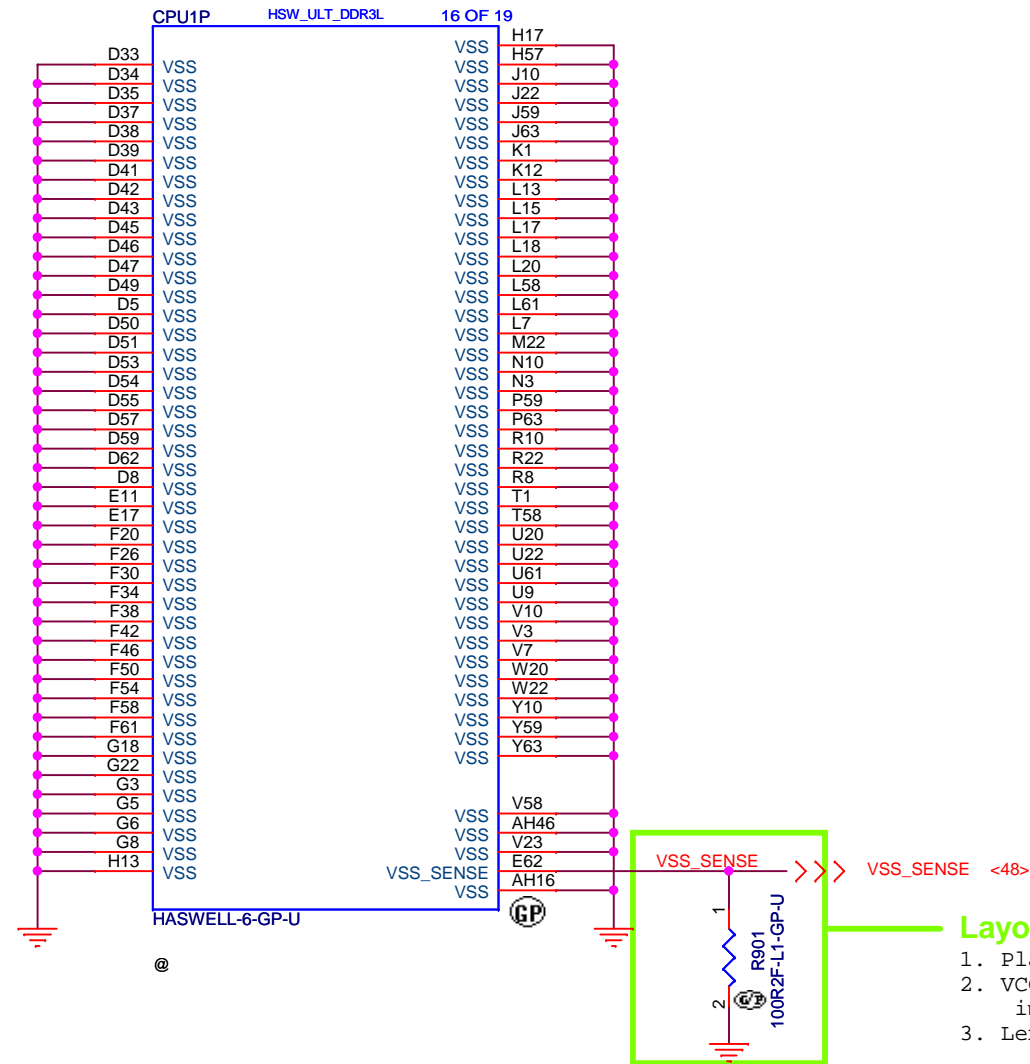
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A



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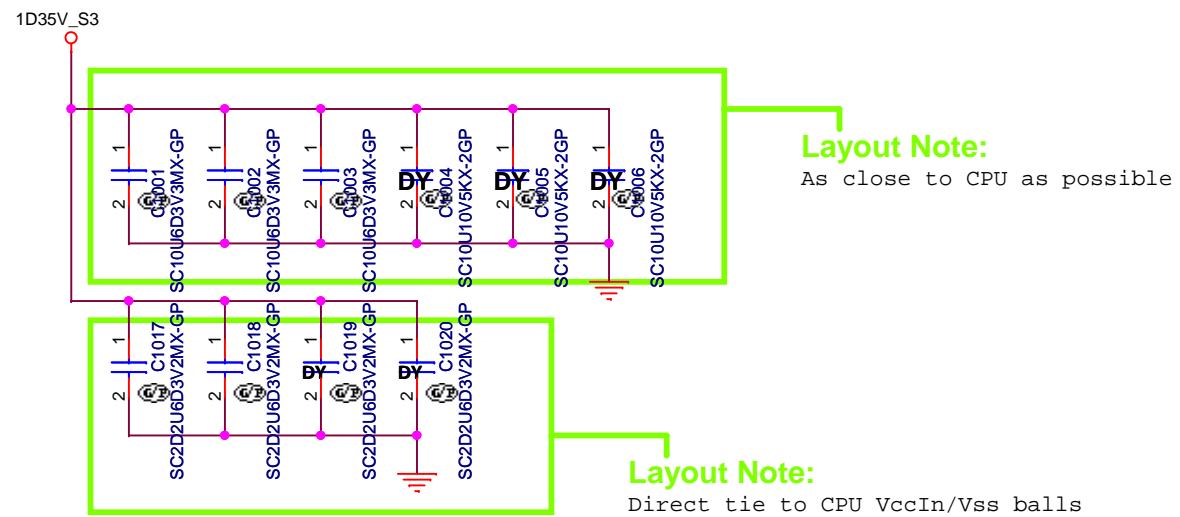
Main Func = CPU



- Layout Note:**
- 1. Place close to CPU
 - 2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
 - 3. Length match<25mil

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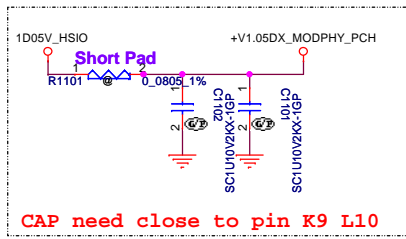
Main Func = CPU



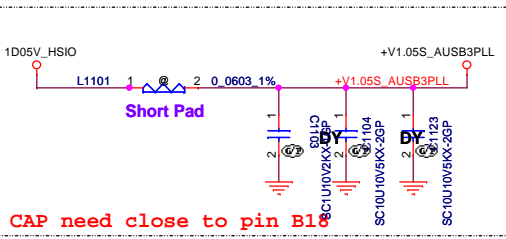
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MAX: 1.92A

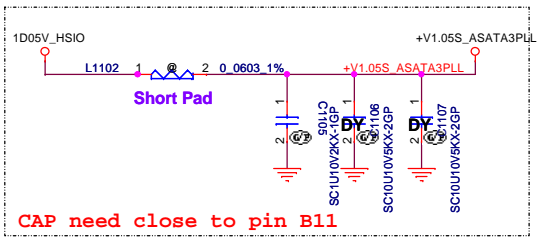
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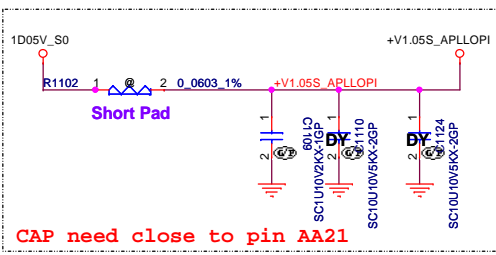
41mA



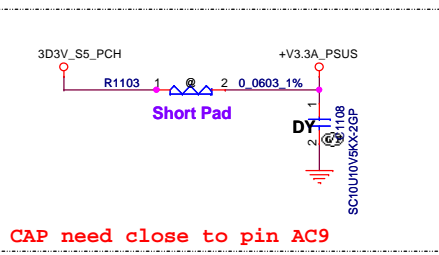
42mA



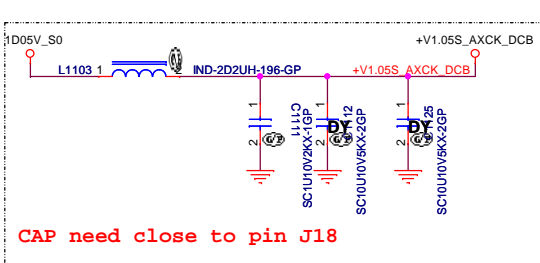
57mA



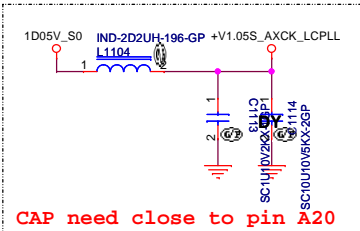
62mA



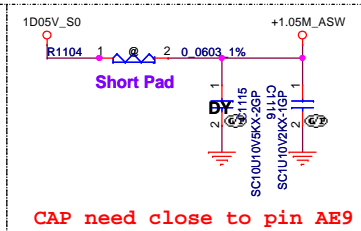
185mA



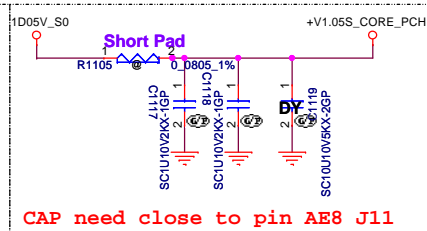
31mA



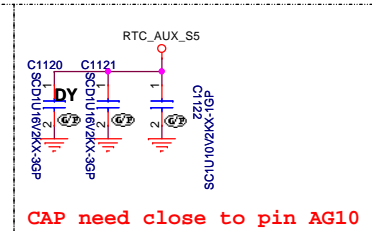
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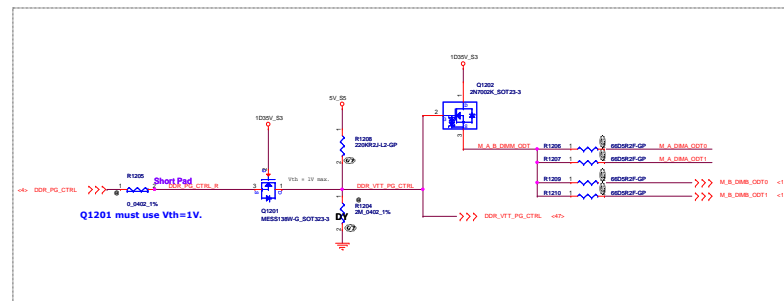
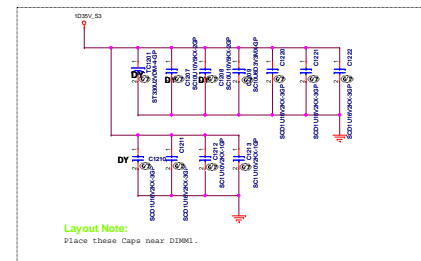
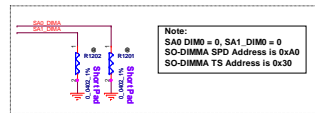
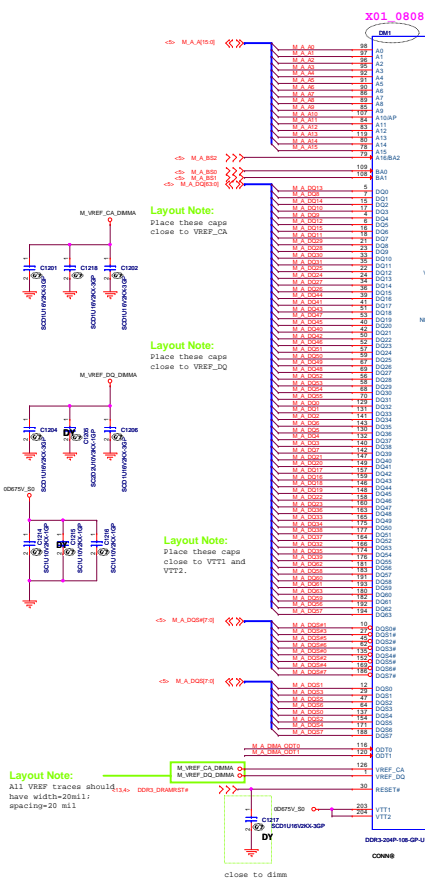


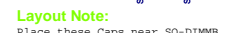
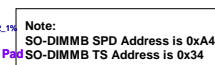
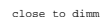
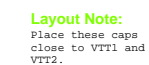
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1mA





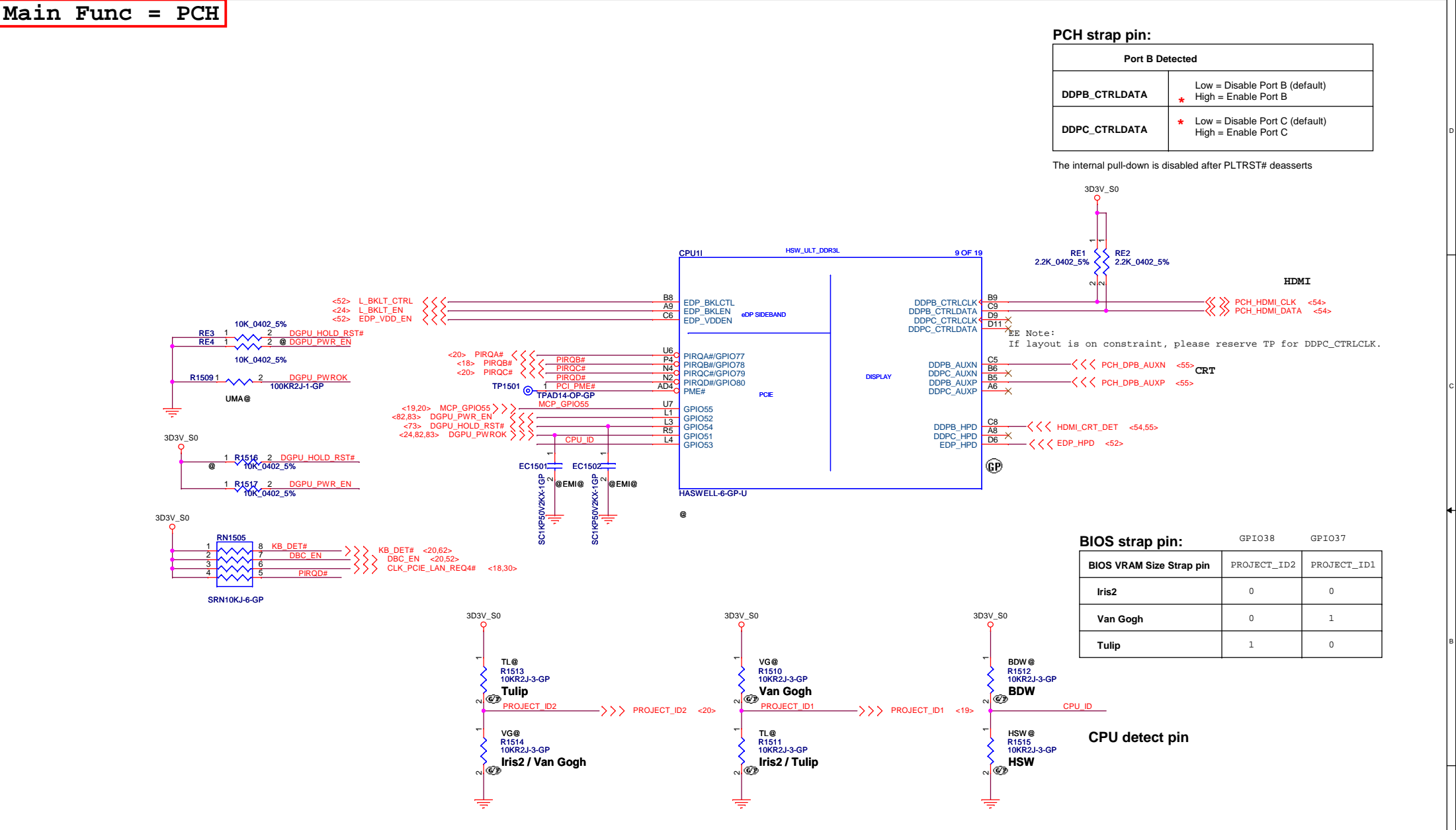


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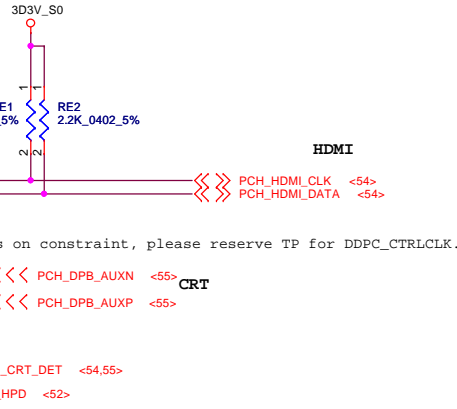
Main Func = PCH



PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	★ Low = Disable Port B (default) High = Enable Port B
DDPC_CTRLDATA	★ Low = Disable Port C (default) High = Enable Port C

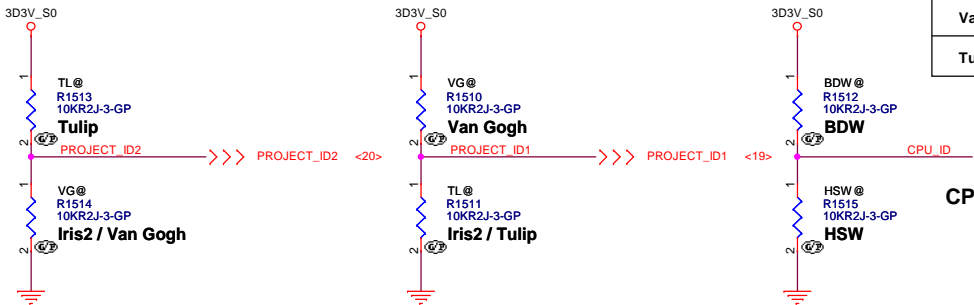
The internal pull-down is disabled after PLTRST# deasserts



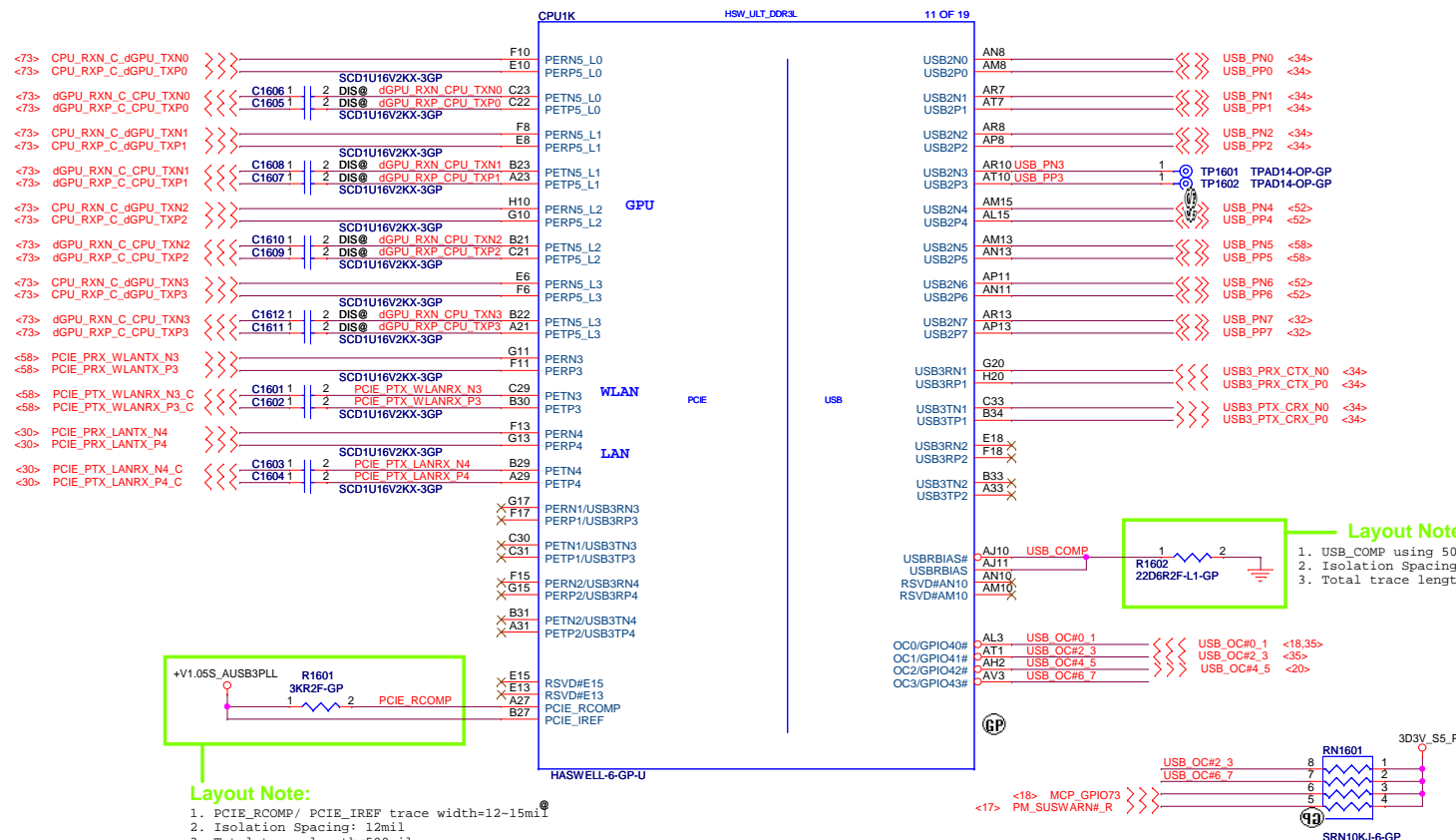
BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2	PROJECT_ID1
Iris2	0	0
Van Gogh	0	1
Tulip	1	0

CPU detect pin



Main Func = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

PCIE Table

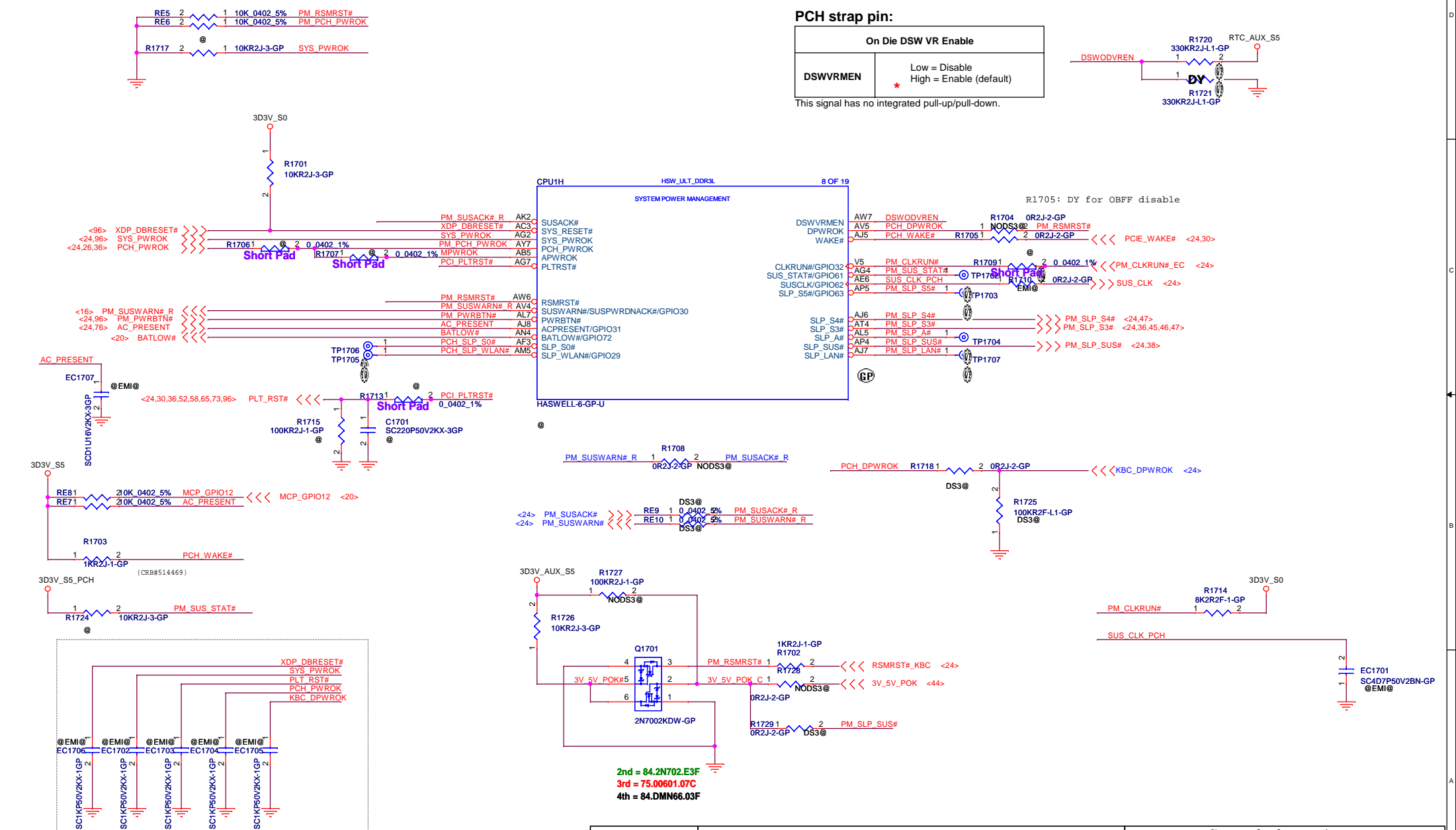
Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU				

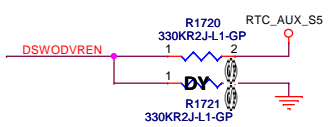
Main Func = PCH



PCH strap pin:

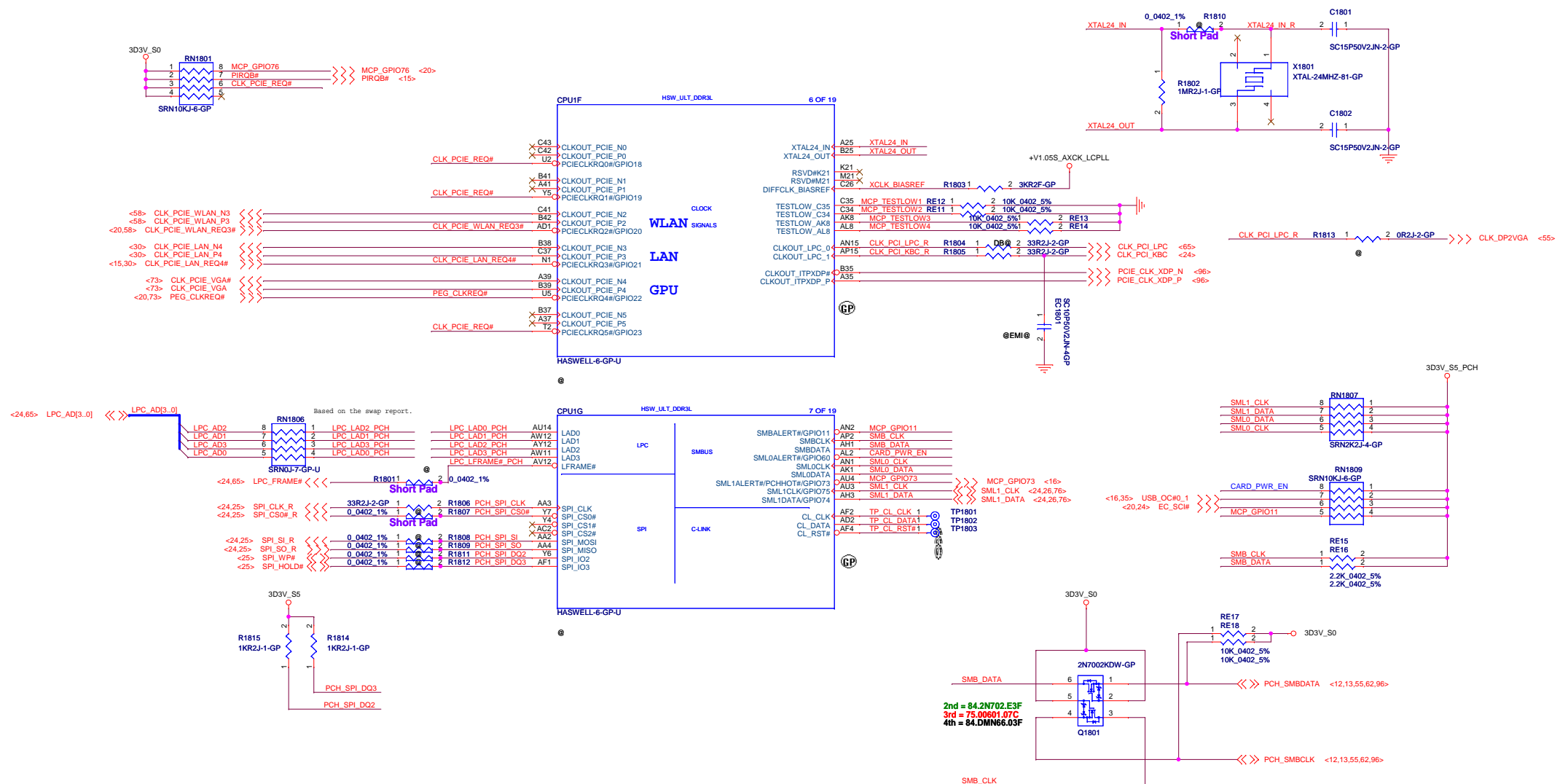
On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default)

This signal has no integrated pull-up/pull-down.



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Main Func = PCH

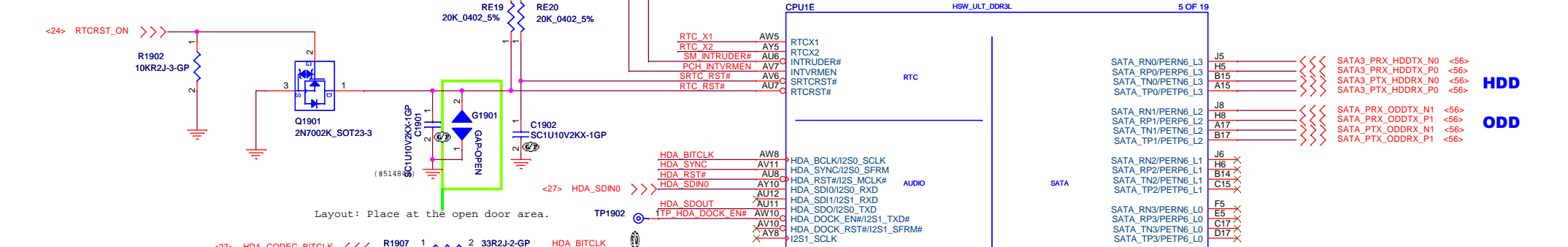


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Main Func = PCH

PCH strap pin:

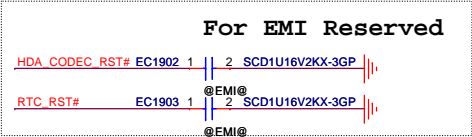
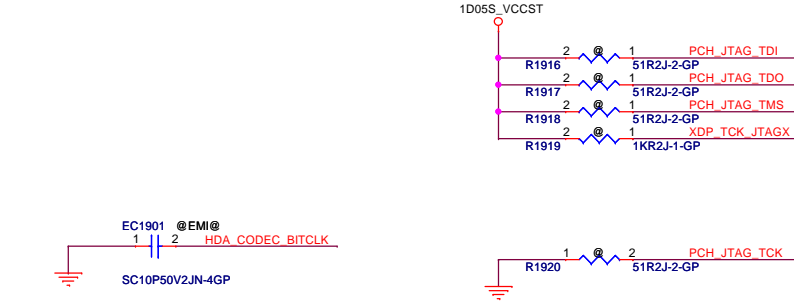
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*



PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

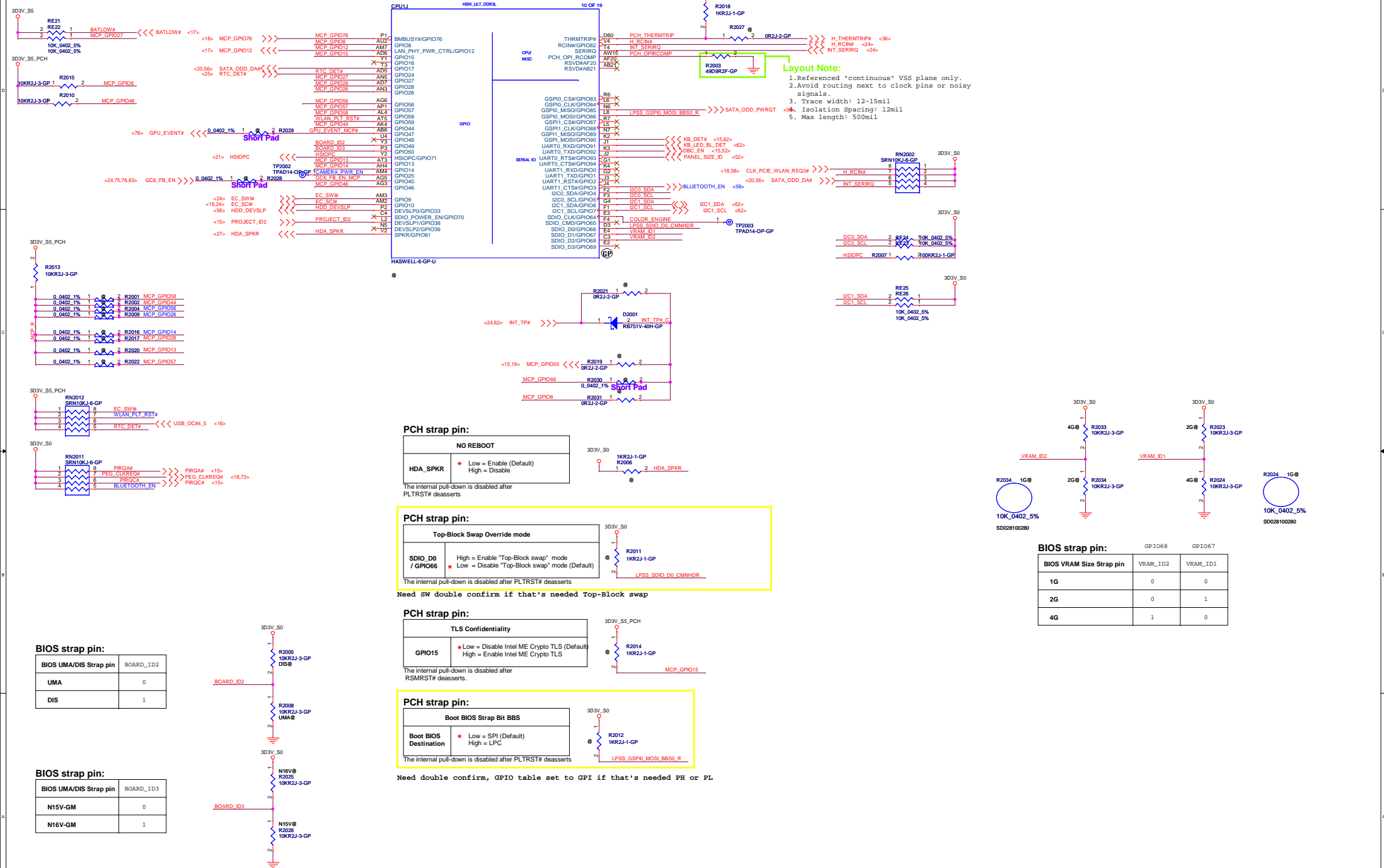


Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.

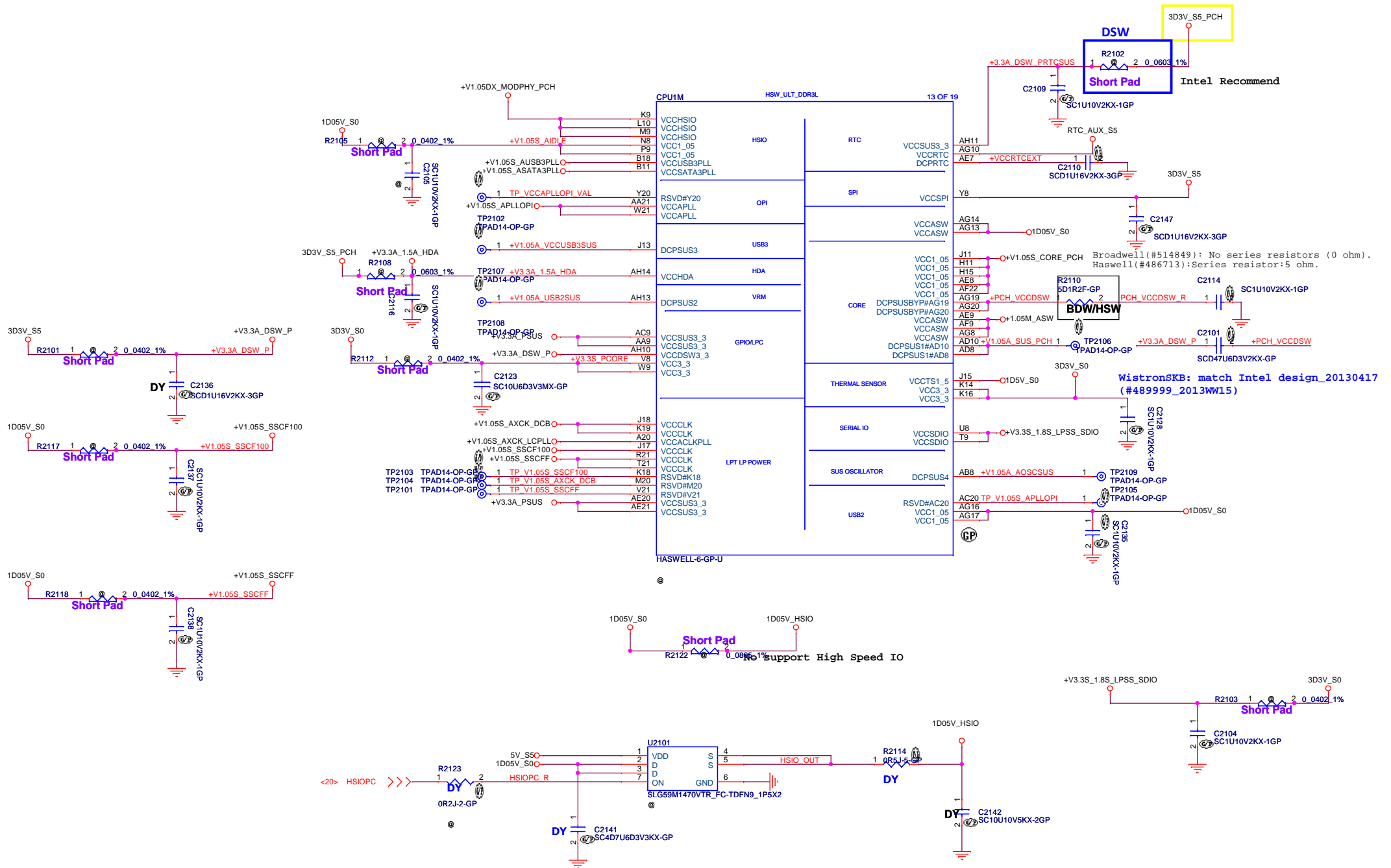
Unused SATA[3:0]GP pins must be terminated to either
3.3V rail or GND using 8.2K to 10K on the
motherboard. Either pull-up or pull-down is acceptable.

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Size	Document Number	Rev		A00	
LA-B483P		Date:		Wednesday, January 21, 2015	
Sheet		19		of 102	

Main Func = PCH

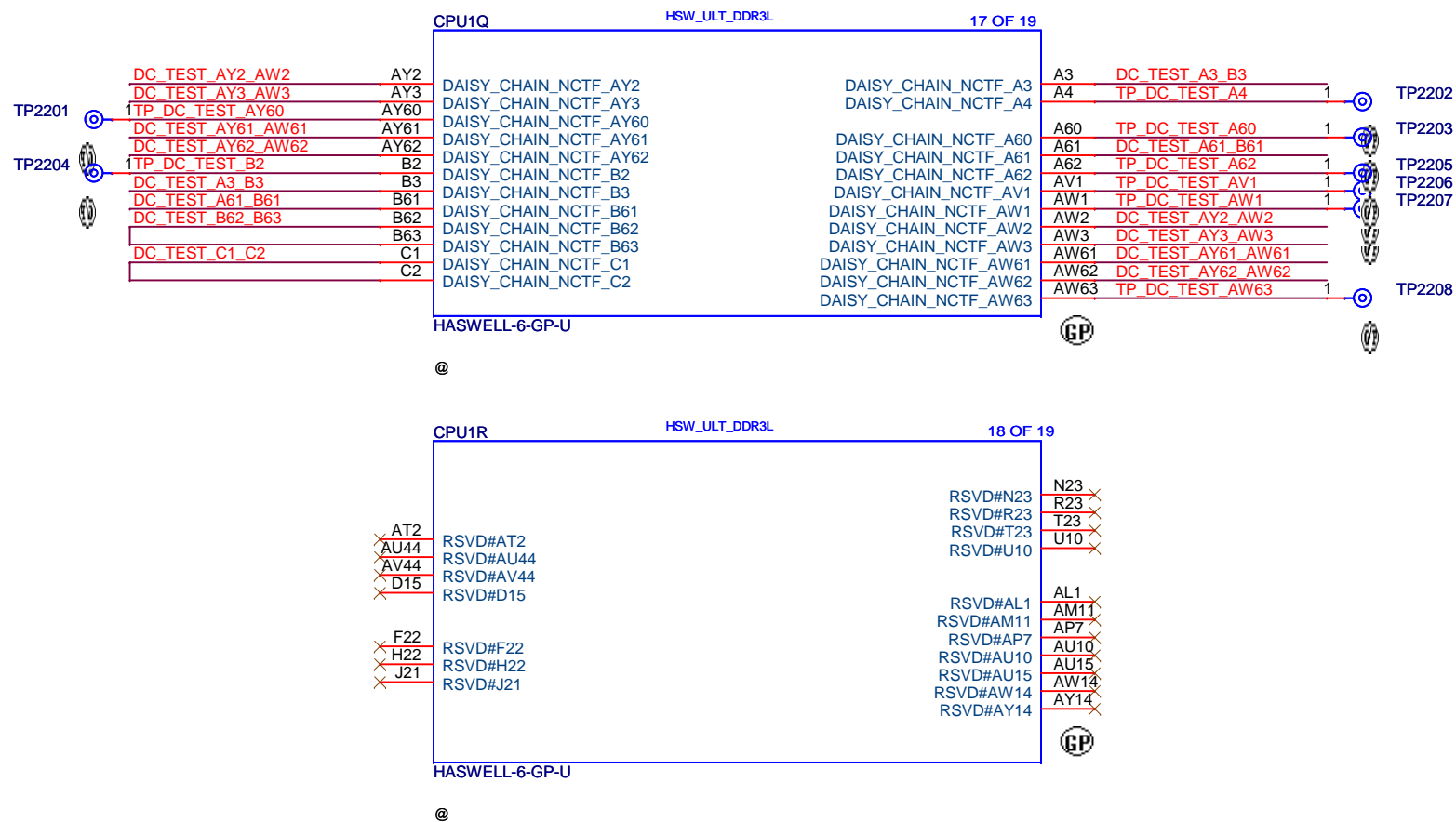


Main Func = PCH



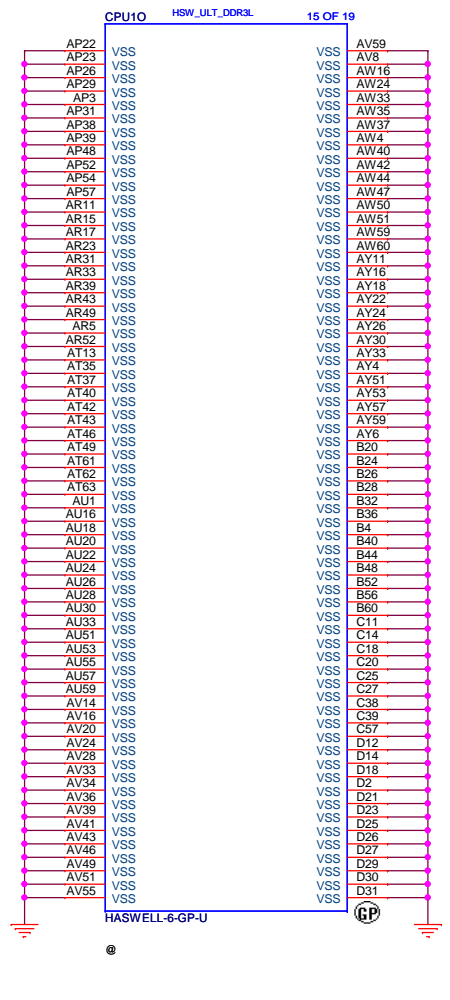
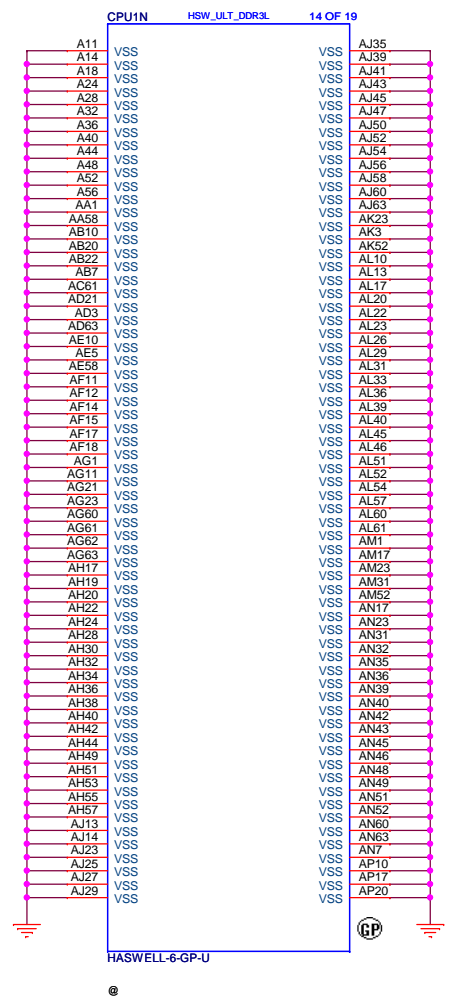
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title CPU (POWER1)		
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					LA-B483P	A00
Date:				Wednesday, January 21, 2015	Sheet	21 of 102

Main Func = PCH

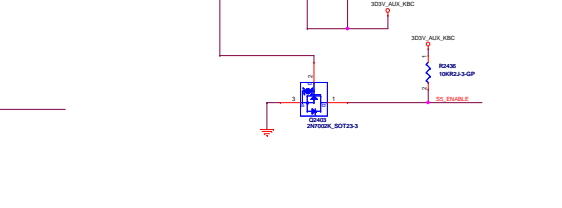
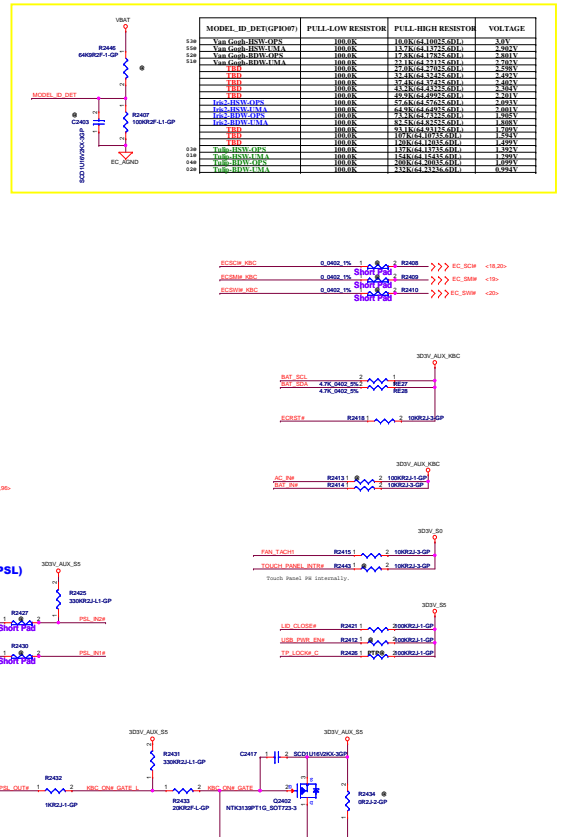


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		Document Number		Rev					
		<i>LA-B483P</i>		A00					
		Date:		Wednesday, January 21, 2015		Sheet		22	

Main Func = PCH

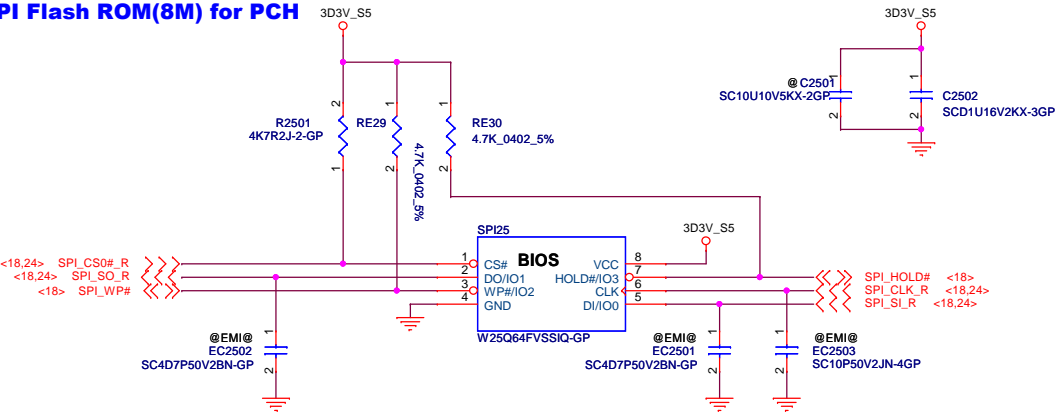


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Date: Wednesday, January 21, 2015		Sheet 23 of 102			



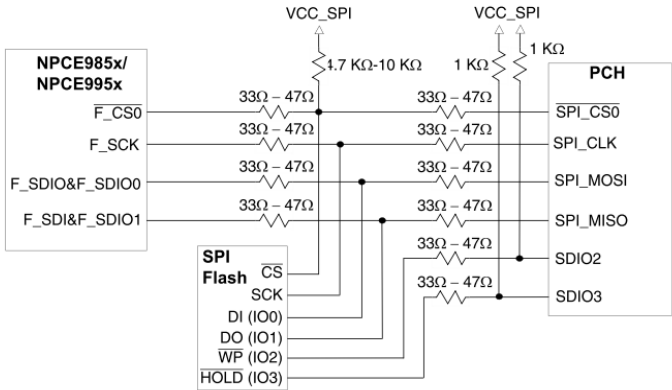
Main Func = SPI Flash

SPI Flash ROM(8M) for PCH



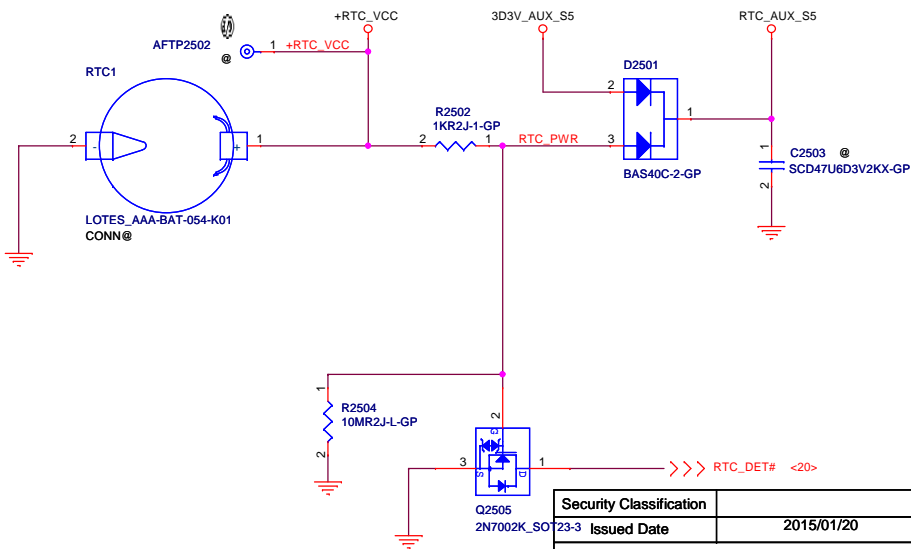
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

Main Func = RTC



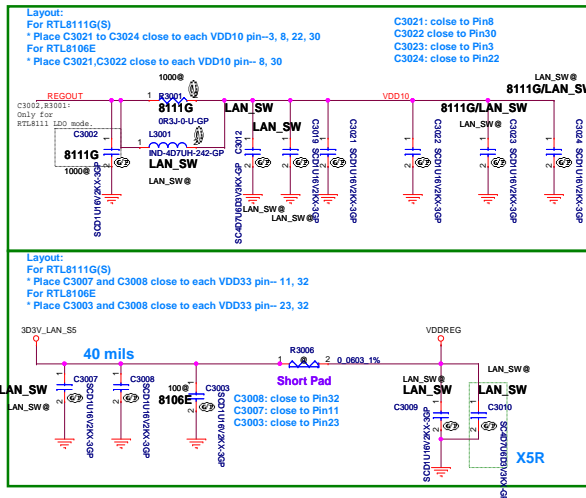
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/01/20				Deciphered Date			
2015/01/20				2015/12/31				Title			
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Date: Wednesday, January 21, 2015				Sheet 25 of 102				Rev A00			

A

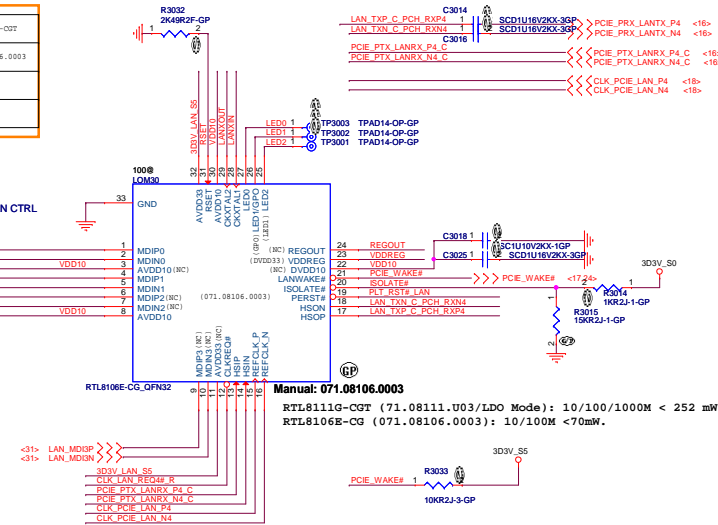
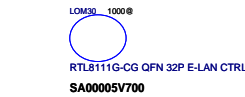
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				Date: Wednesday, January 21, 2015	Rev A00
				Document Number	
				LA-B483P	
				Sheet 28 of 102	

LAN CHIP (10/100/1000M & 10/100M co-lay)

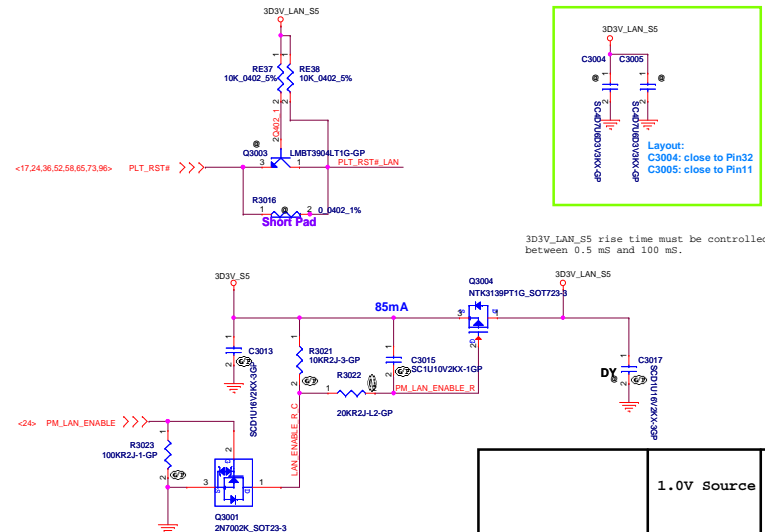


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CGT
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M




Manual: 071.08106.0003

RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M <70mW.

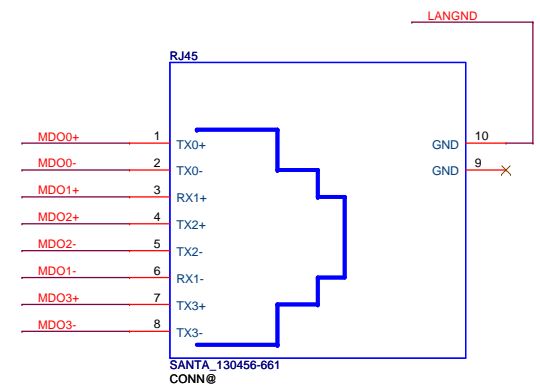
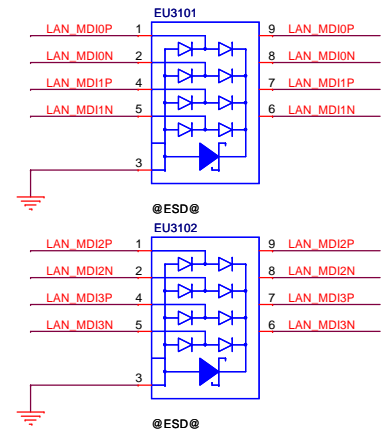
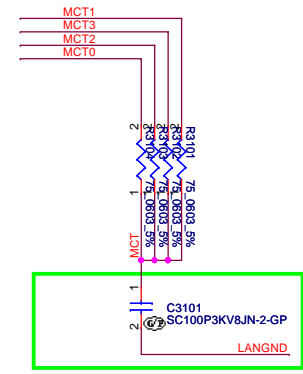
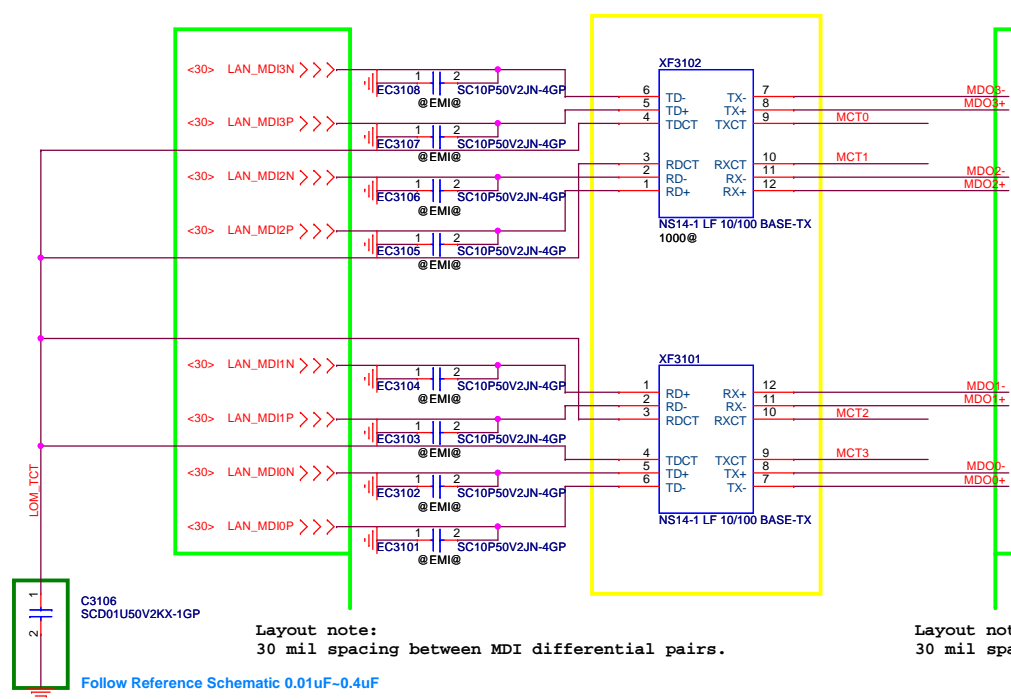


3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.

[illegible]

Security Classification	Compal Secret Data			
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title
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Date:	Y20160121		Sheet	30 of 102

LAN TransFormer (10/100/1000M & 10/100M co-lay)

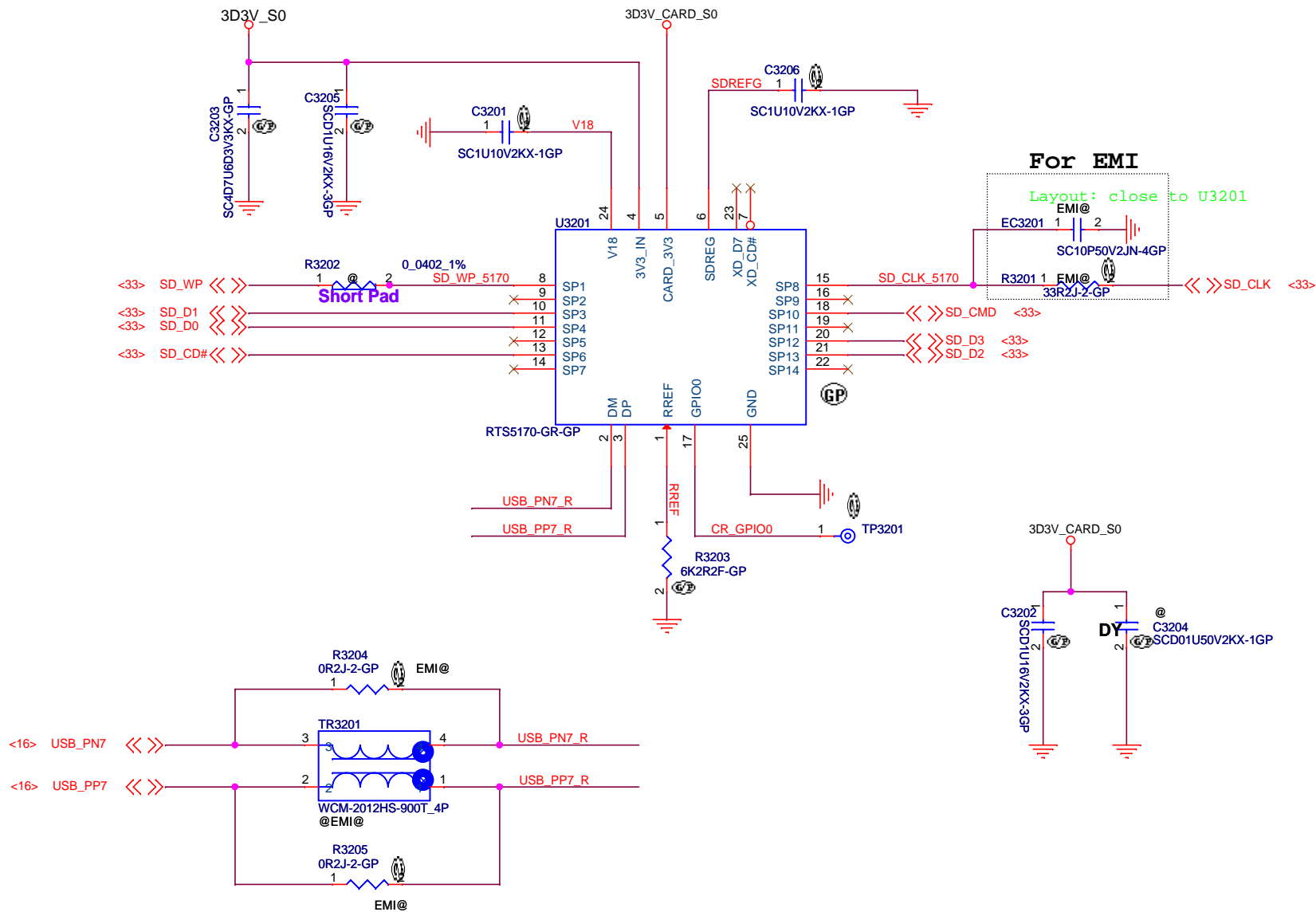


Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.

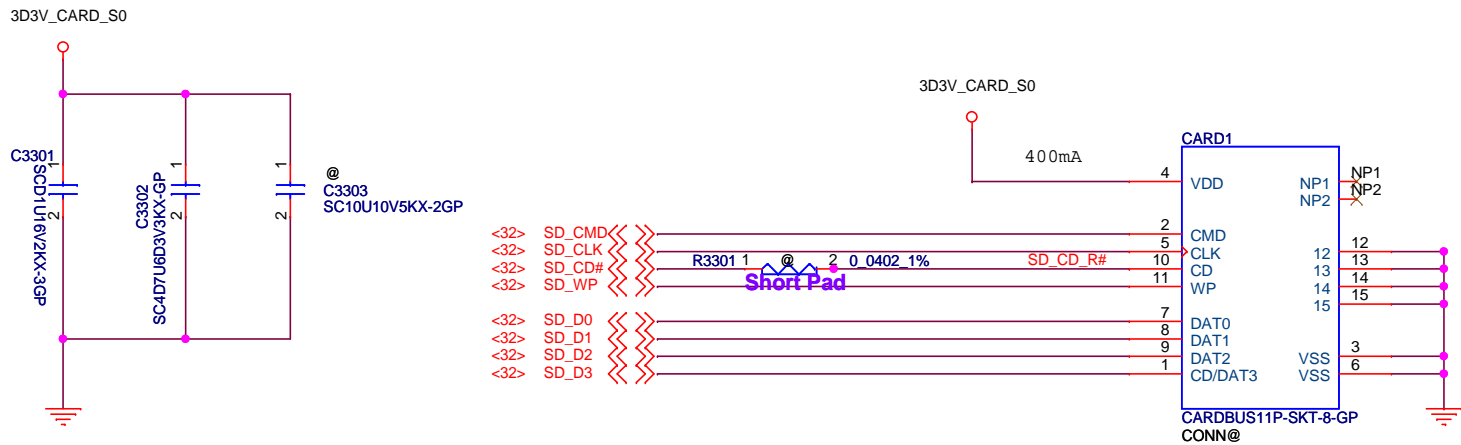
Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

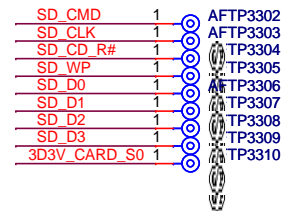
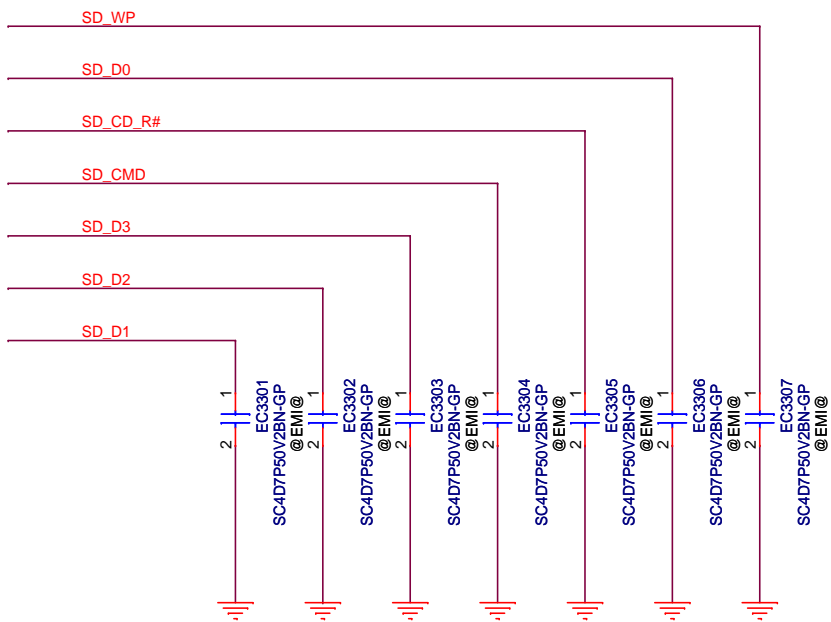


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Main Func = Card Reader



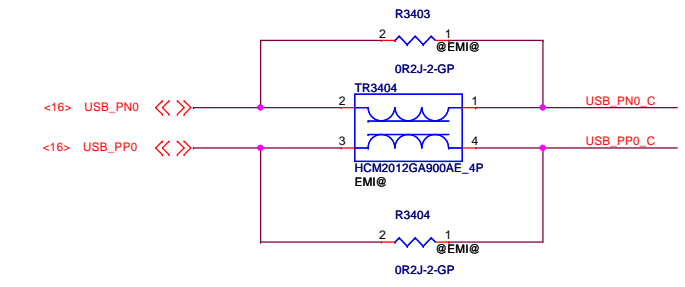
For EMI Reserved



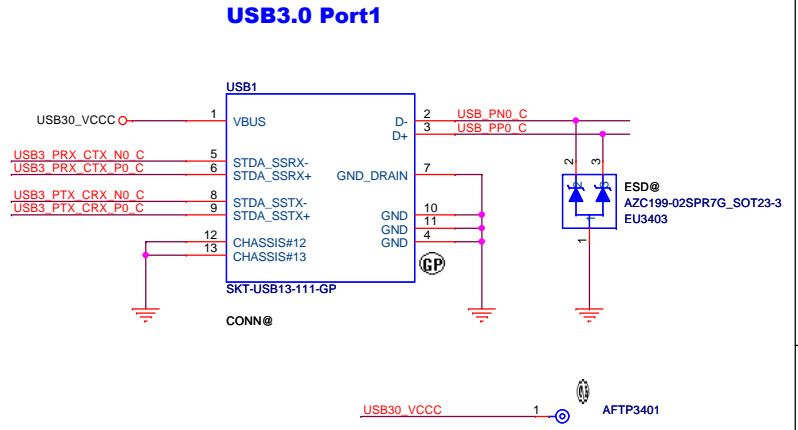
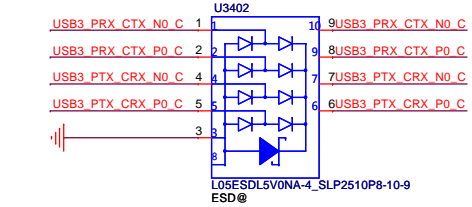
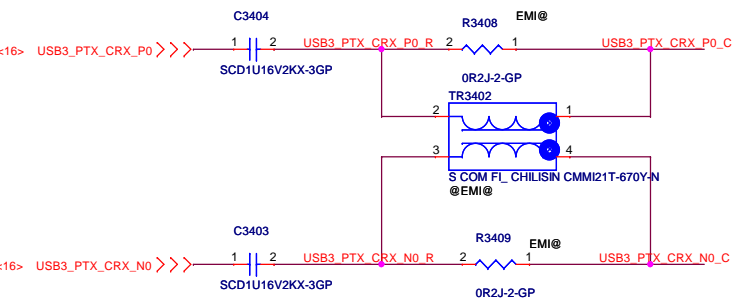
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Size		Document Number			Rev
		LA-B483P			A00
Date:		Wednesday, January 21, 2015		Sheet	33 of 102

Main Func = USB3.0 Port1

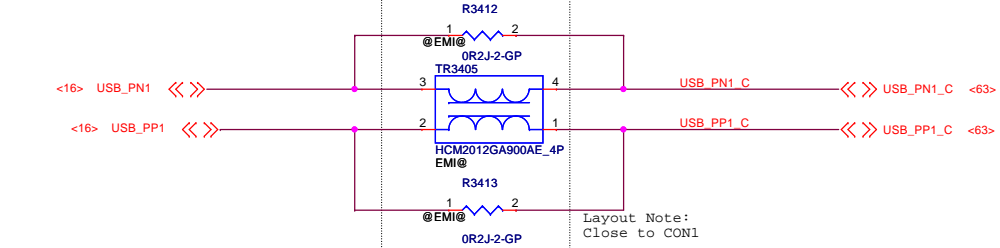
USB2.0 Port2 and USB2.0 Port3 are on IOBD



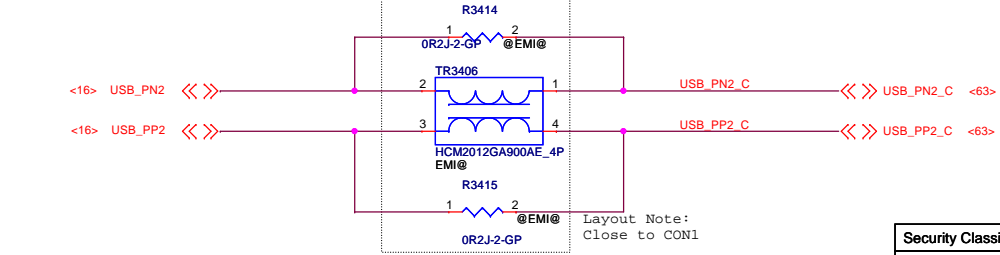
USB2.0/3.0 filter use SM070003Q00



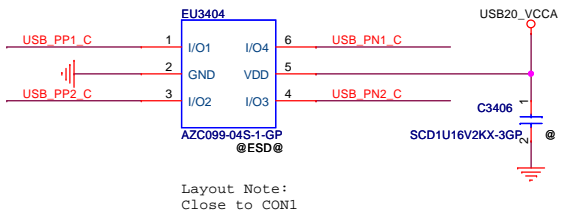
USB2 (USB2.0) CMC



USB3 (USB2.0) CMC

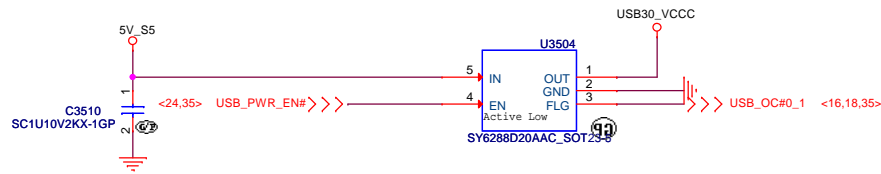


USB ESD Diode



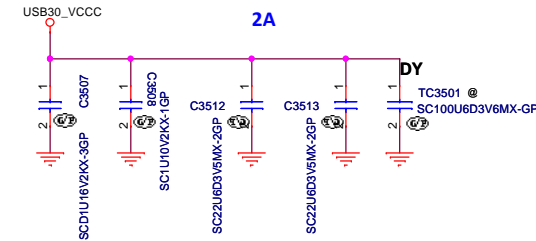
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	
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				Document Number	
				Rev	
				Date	
				Sheet	
				of	
				102	

Main Func = USB3.0 Port1



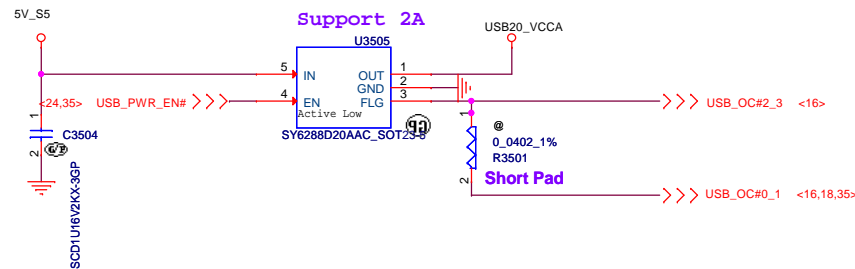
USB3.0 Port1

Layout Note: Close USB1



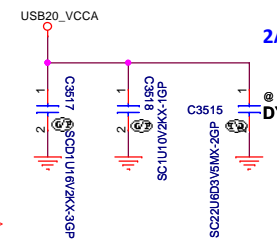
Main Func = USB2.0 Port2

Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)

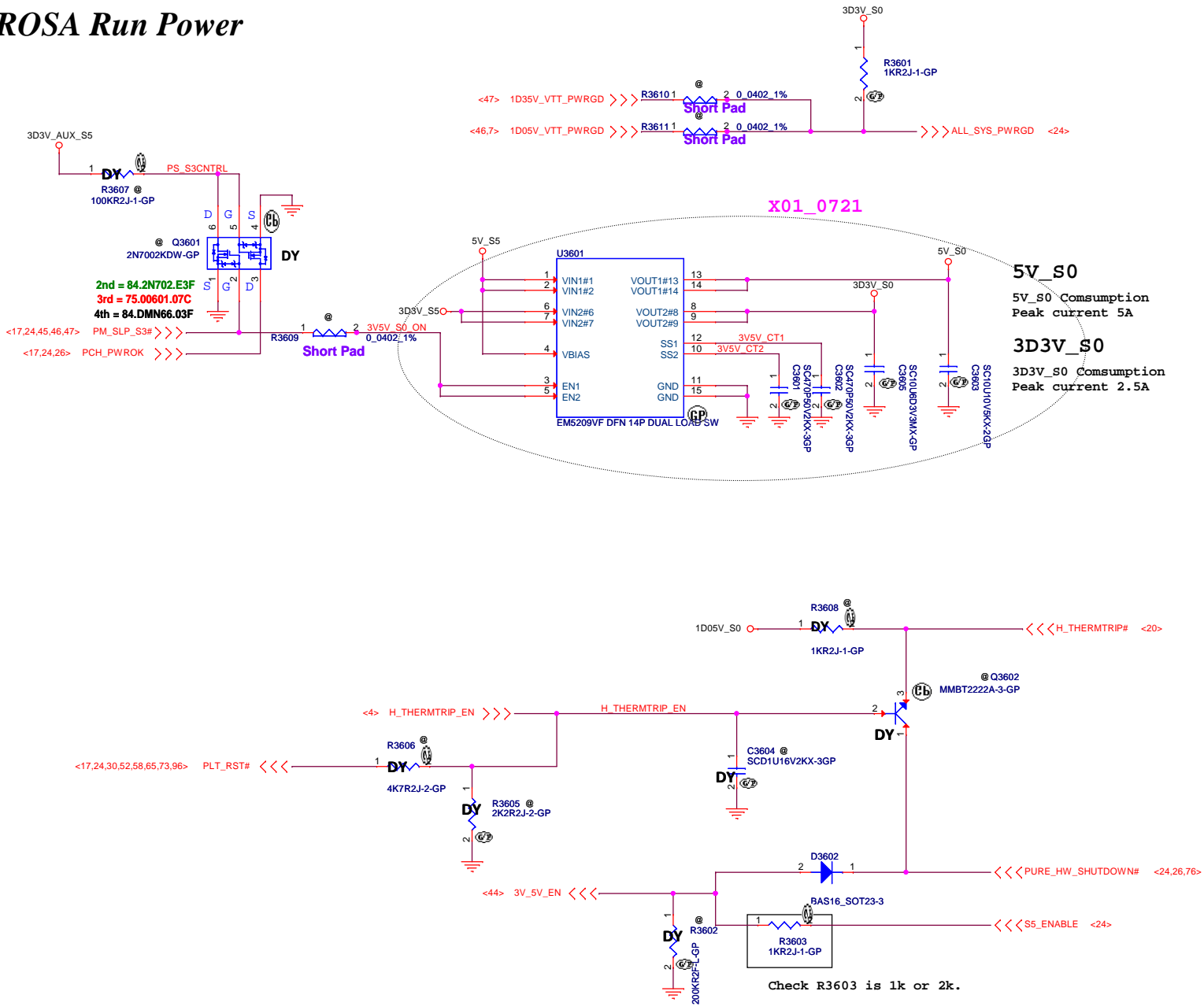
Layout Note: Close CON1



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				Date	Wednesday, January 21, 2015
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				Rev	A00

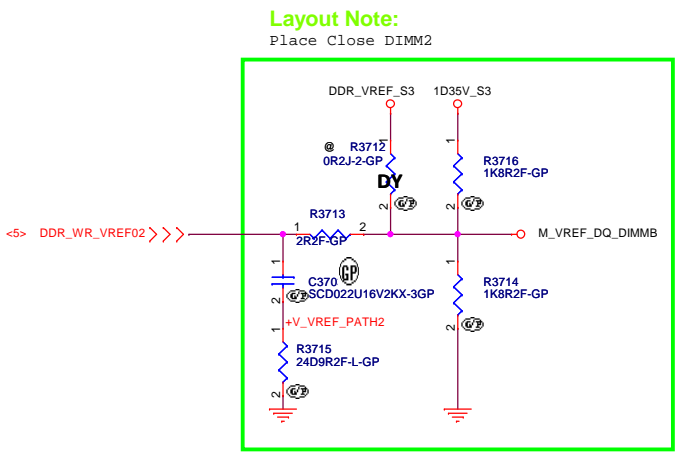
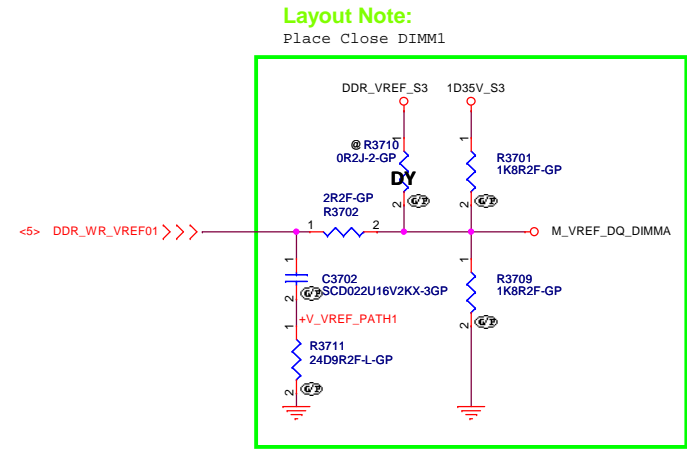
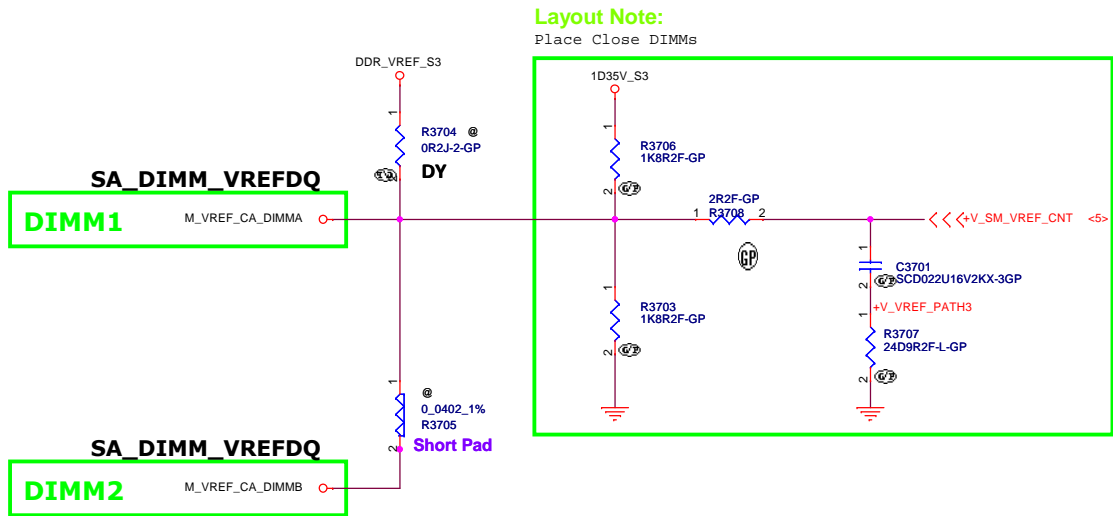
Power Good

ROSA Run Power



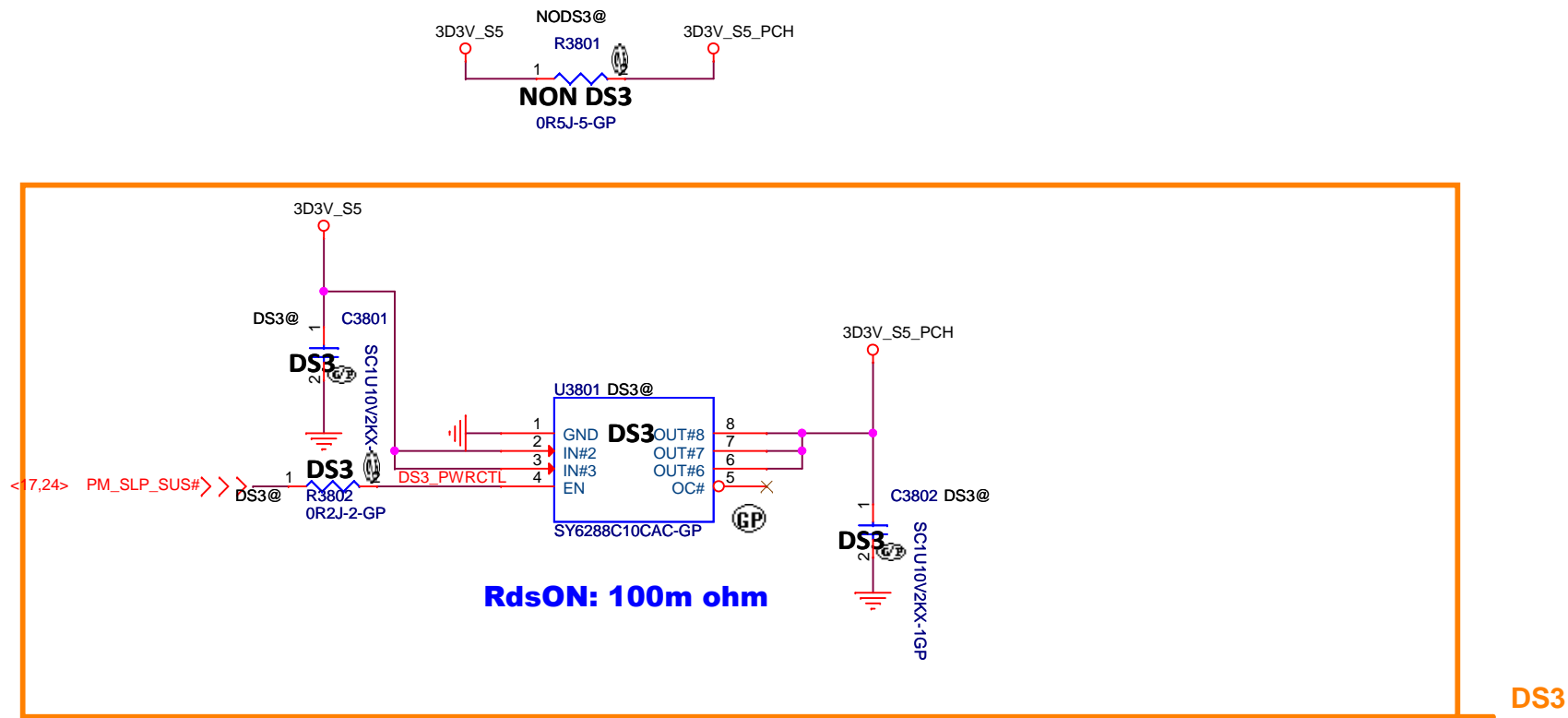
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2015/01/20		Title	
		Deciphered Date		Power Plane Enable	
		2015/12/31		Size	
				Document Number	
				LA-B483P	
				Date	
				Wednesday, January 21, 2015	
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				102	
				Rev	
				A00	

Main Func = DIMM1
Main Func = DIMM2



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Main Func = Power Plane & Sequence



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Date: Wednesday, January 21, 2015		Sheet 38 of 102			

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						Document Number		Rev	
						LA-B483P		A00	
						Date: Wednesday, January 21, 2015		Sheet 39 of 102	

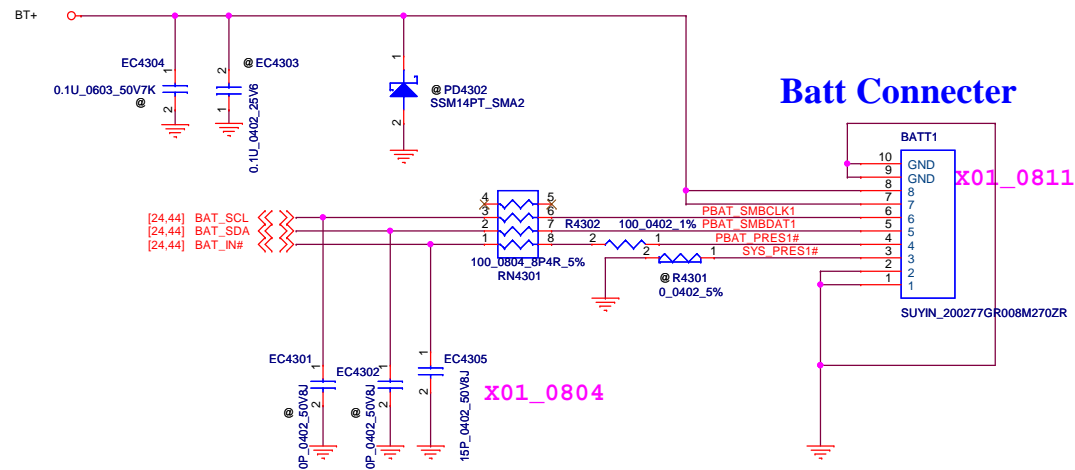
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title		
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				Document Number	Rev	
				<i>LA-B483P</i>		A00
				Date:	Wednesday, January 21, 2015	Sheet 40 of 102

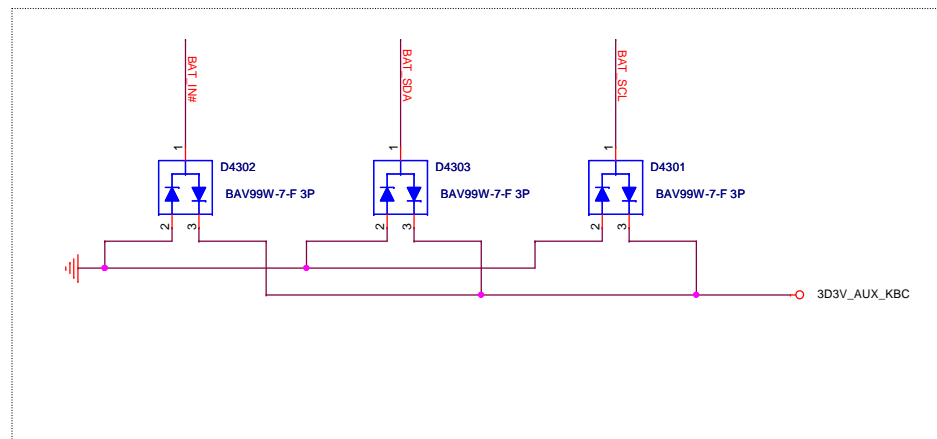
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						Document Number		Rev	
						LA-B483P		A00	
						Date:		Wednesday, January 21, 2015	

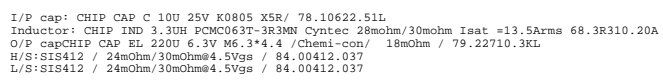
Main Func = M-BAT Input



Placement: Close to Batt Connector

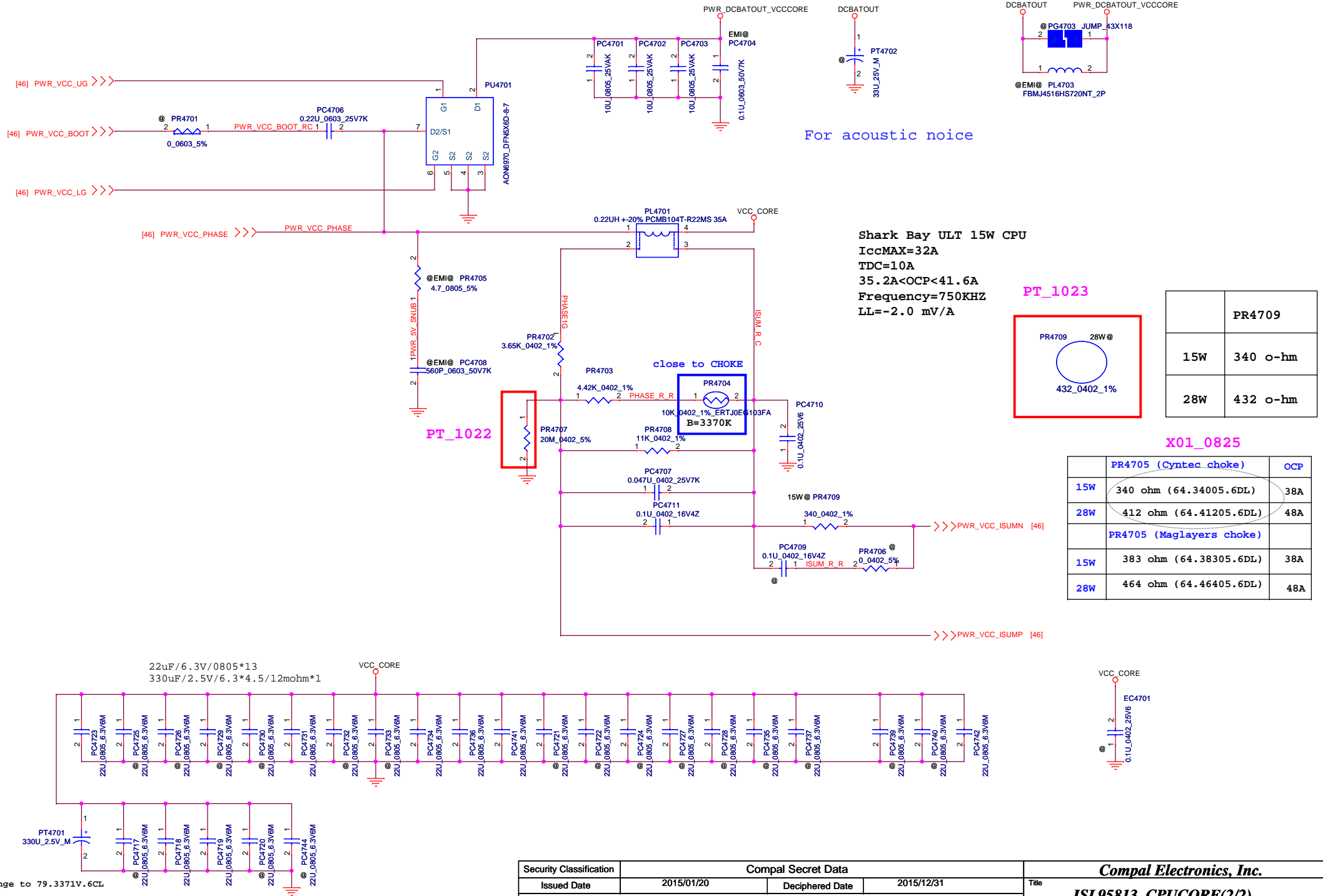


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				Rev	A00

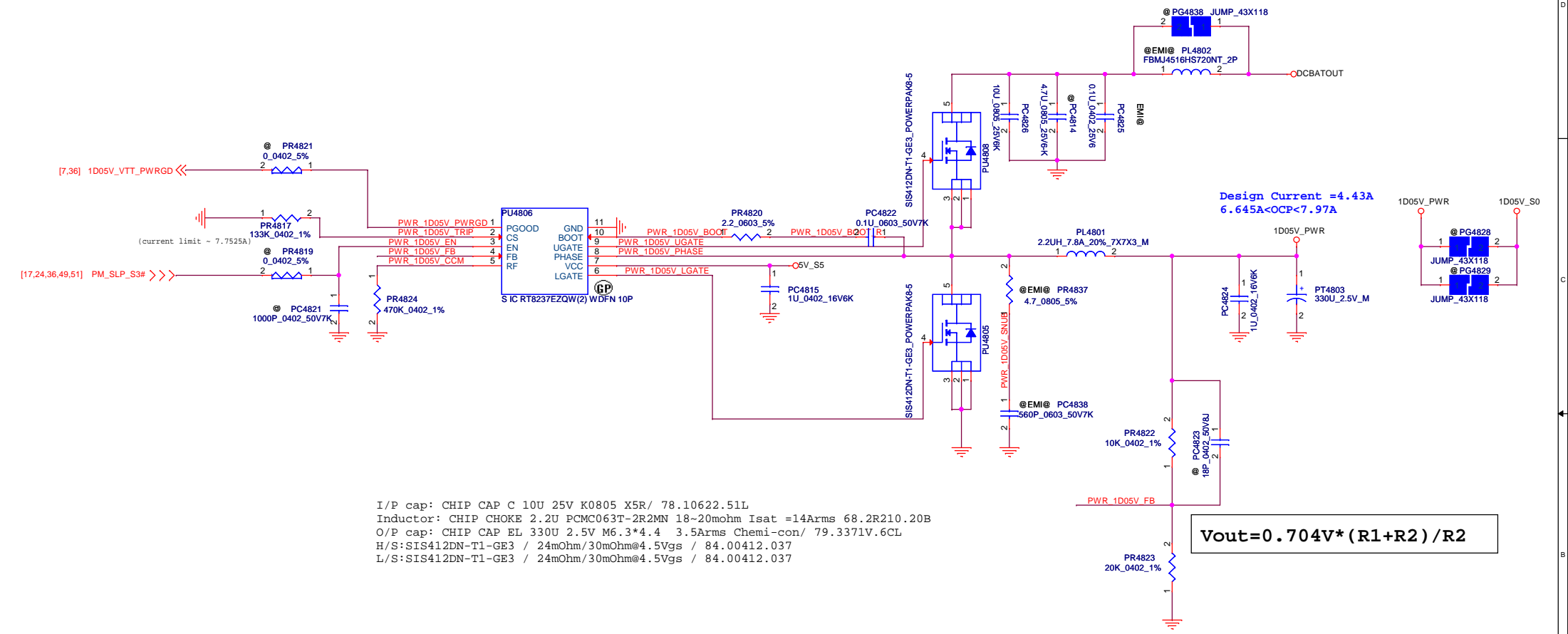


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			TPS51225 5V/3D3V	400
			Doc. Number	
			LA-B483P	

Main Func = CPU_CORE



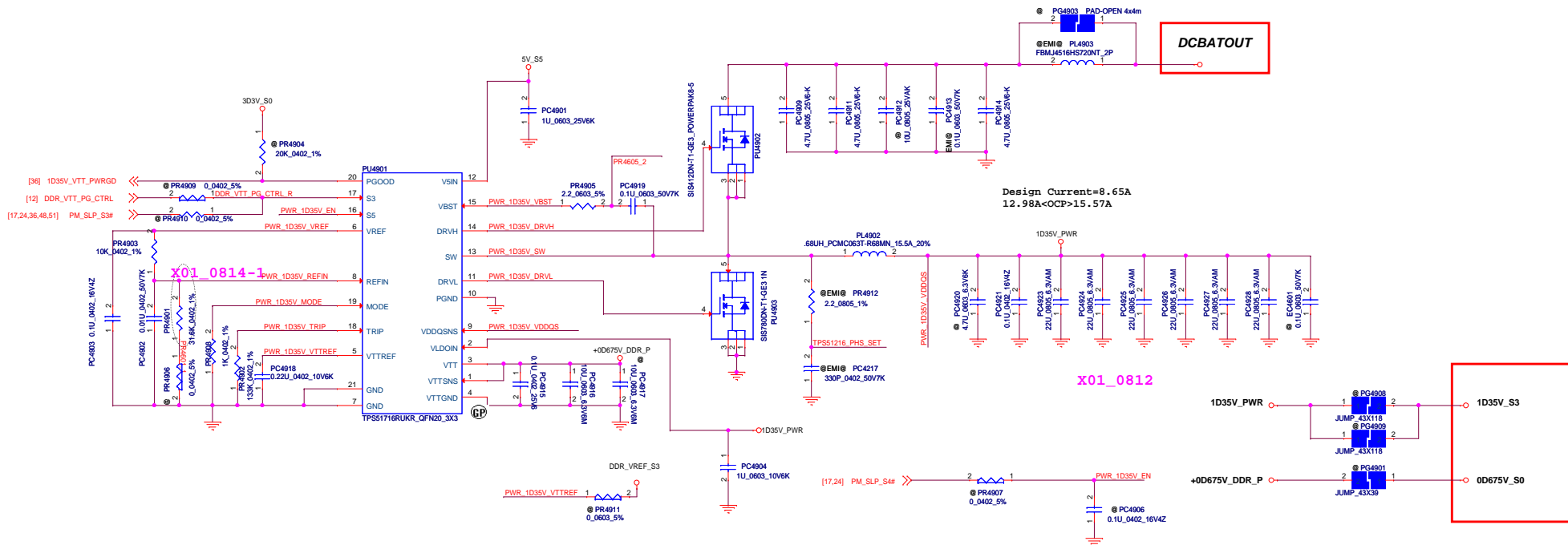
Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

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Size		Document Number		Rev	
		LA-B483P		A00	
Date:		Wednesday, January 21, 2015		Sheet 48 of 102	



State	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

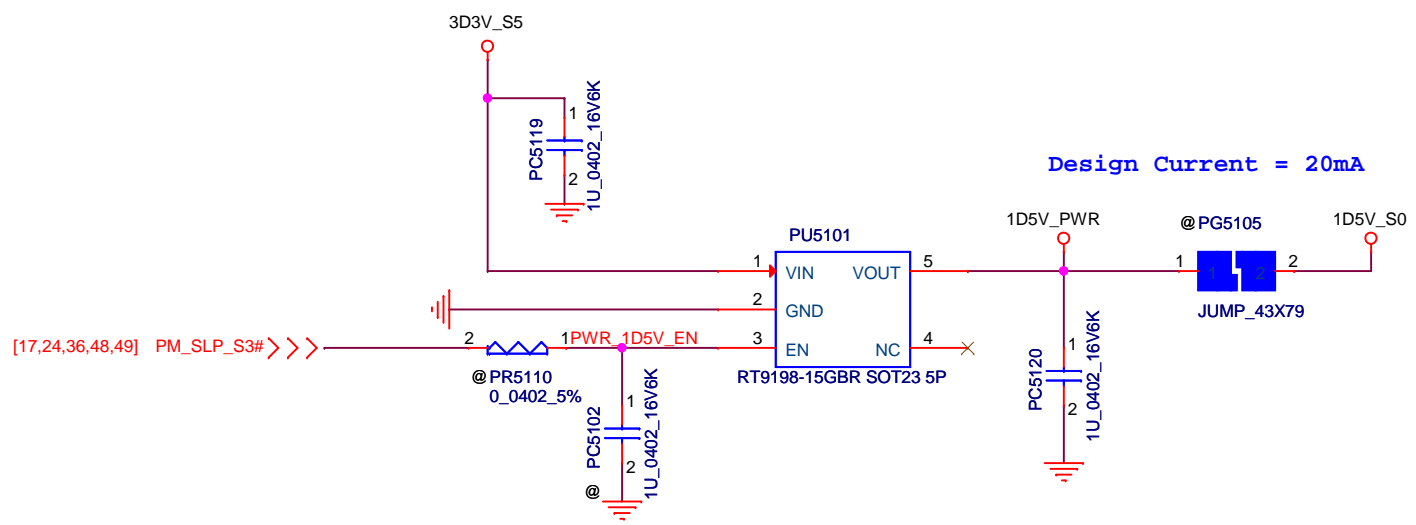
I/P cap: 10U 25V K0805 X5R / 78.10622.51L
Inductor: CHIP CHOKR 1.5U PCMC0637-1R5MN 14-15mohm Isat =18Arms 68.1R510.10K
O/P cap: CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
H/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Component	VRAM 4pcs (design current=8.65A)	VRAM 8pcs (design current=10.5A)	
PR4902	133K 64.13335.6DL	191K 64.19135.6DL	OCP setting
PC4927	DV	Stuiff	output MLCC
PC4928	DV	Stuiff	output MLCC

(Blanking)

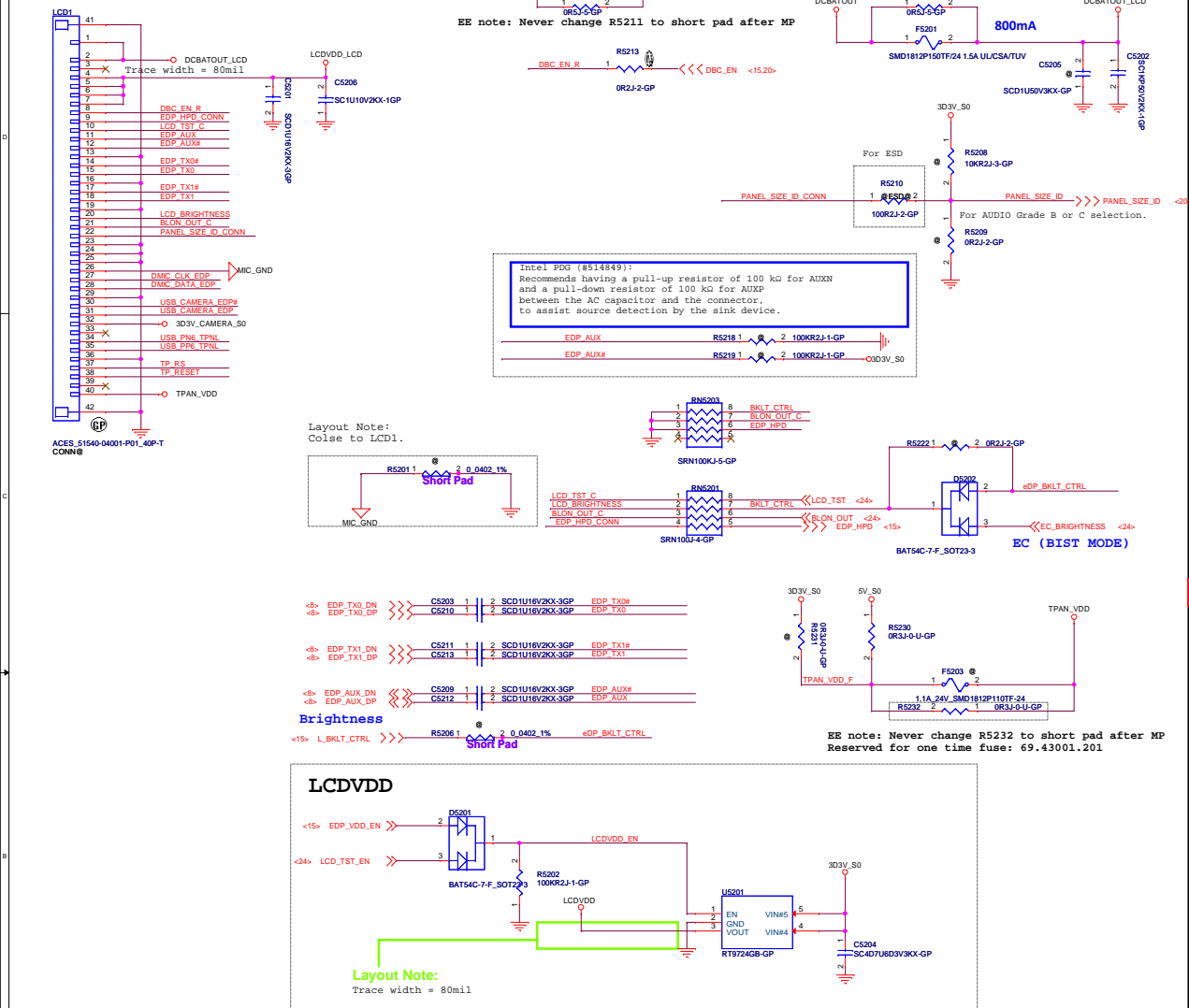
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Main Func = 1D5V

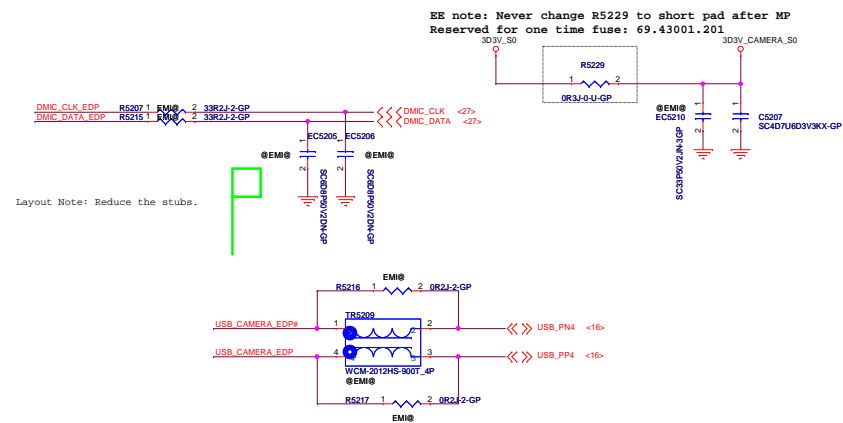


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				Document Number	Rev	
				LA-B483P		A00
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Main Func = LCD

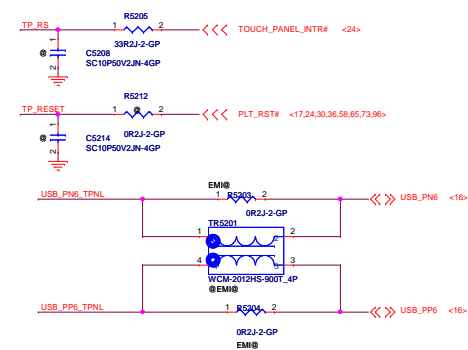


Main Func = CAM



Main Func = TS

Touch Panel

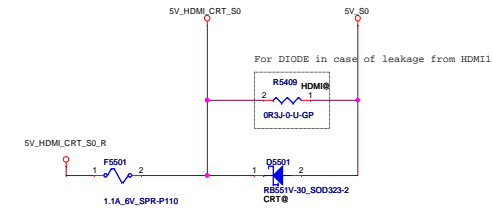
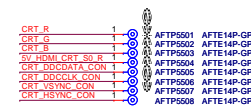
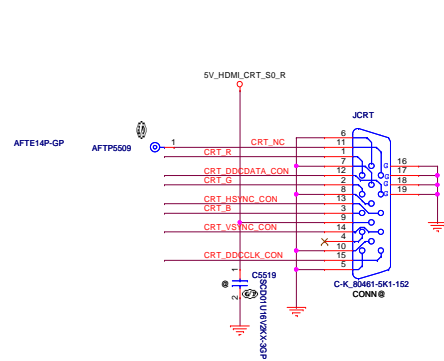


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				Rev	A00
				Date	Thursday, January 22, 2015
				Sheet	52 of 102

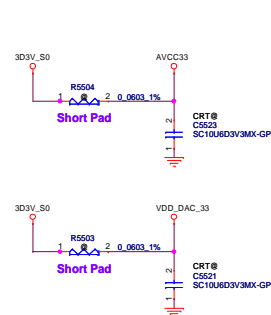
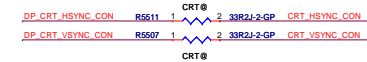
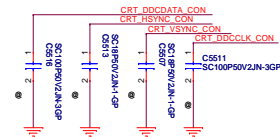
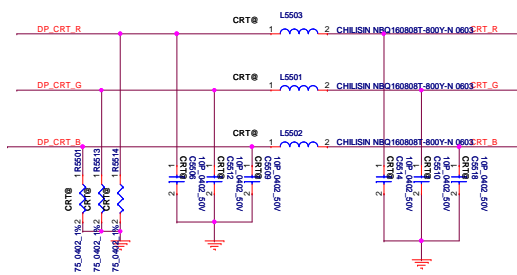
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				Size	Document Number	Rev
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				Date:	Wednesday, January 21, 2015	Sheet 53 of 102

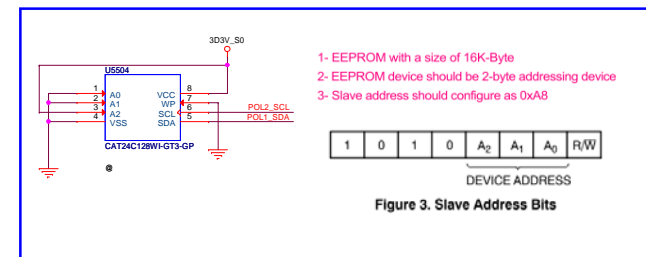
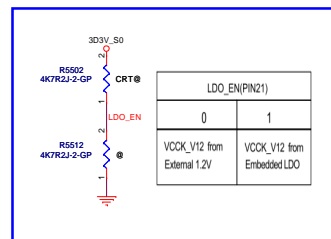
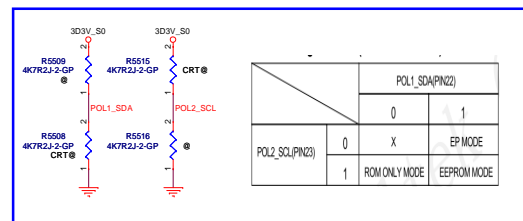
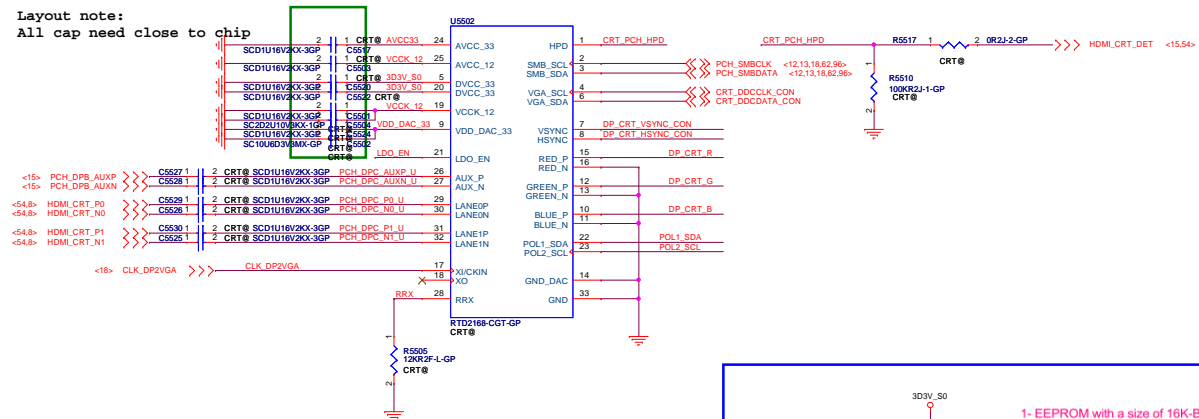
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



CRT RGB
CRT H/VSYNC
CRT SMBUS



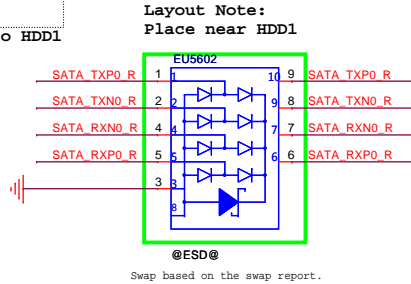
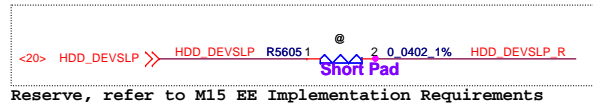
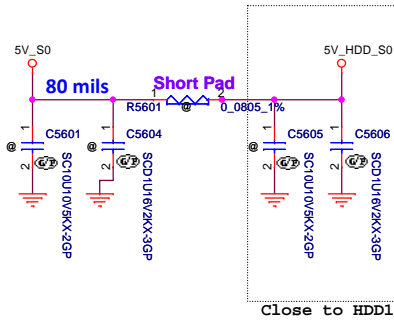
Layout note:
All cap need close to chip



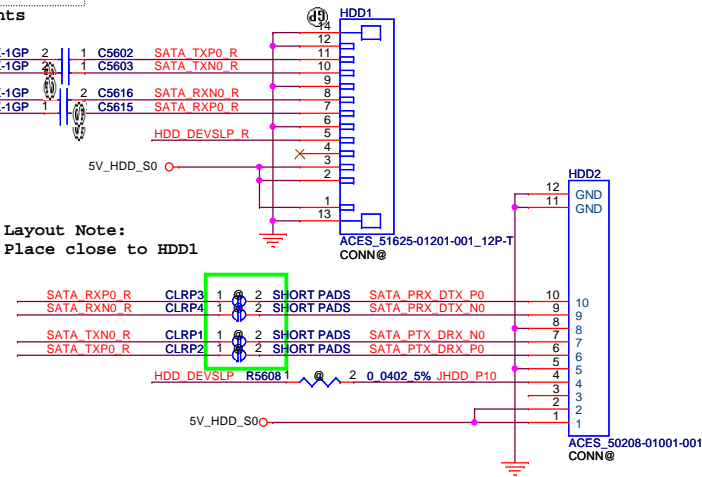
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Main Func = HDD

SATA HDD Connector



Layout Note:
Place close to HDD1

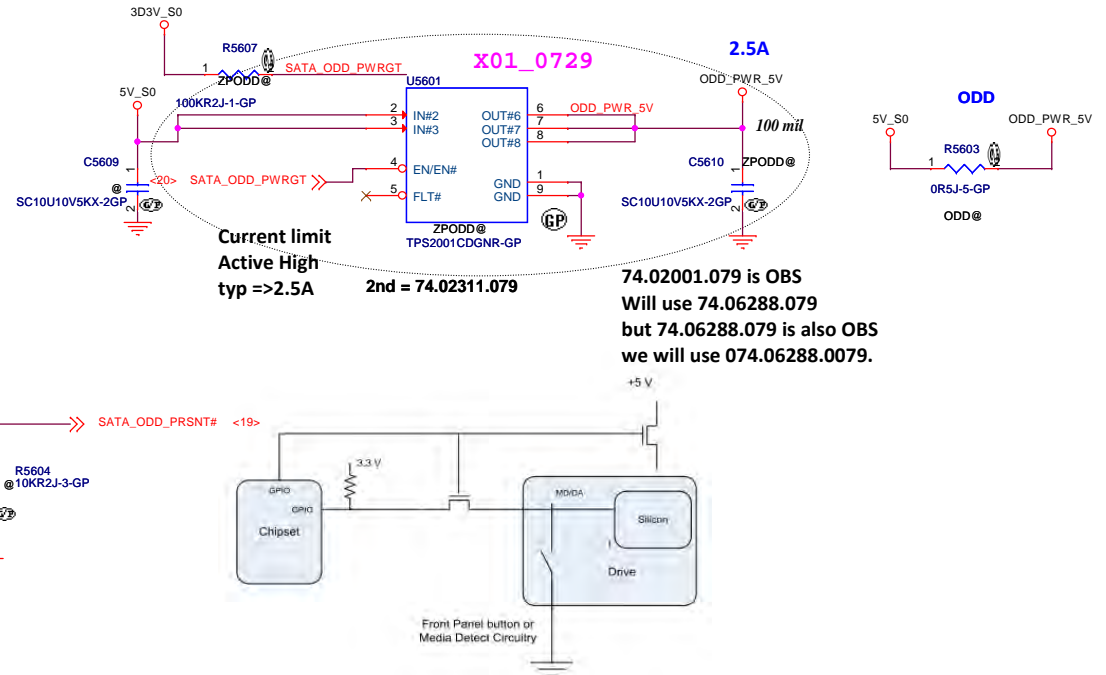
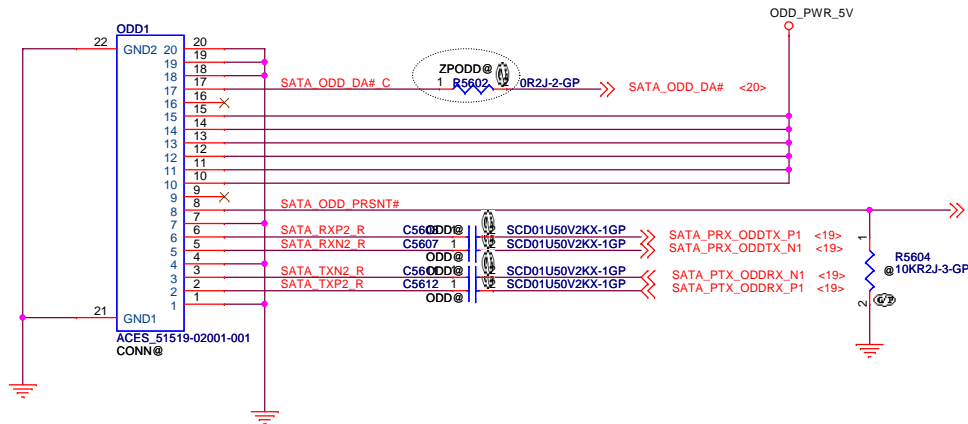


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

SATA Zero Power ODD

ODD Connector



74.02001.079 is OBS
Will use 74.06288.079
but 74.06288.079 is also OBS
we will use 074.06288.0079.

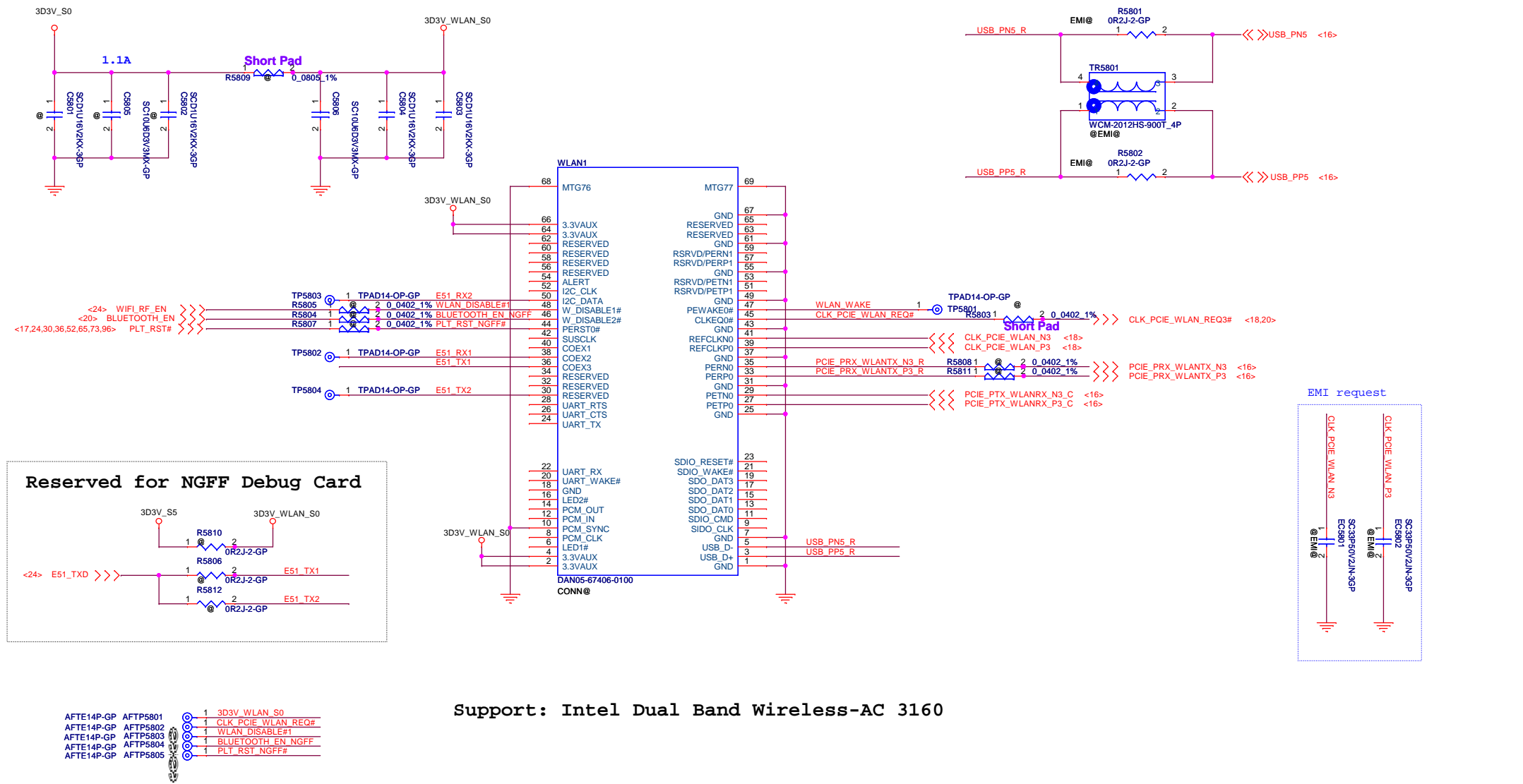
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	HDD/ODD
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SSID = ESATA

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Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

- AFTE14P-GP AFTP5801 1 3D3V WLAN_S0
- AFTE14P-GP AFTP5802 1 CLK_PCIE_WLAN_REQ#
- AFTE14P-GP AFTP5803 1 WLAN_DISABLE#1
- AFTE14P-GP AFTP5804 1 BLUETOOTH_EN_NGFF
- AFTE14P-GP AFTP5805 1 PLT_RST_NGFF#

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					NGFF WLAN CONN
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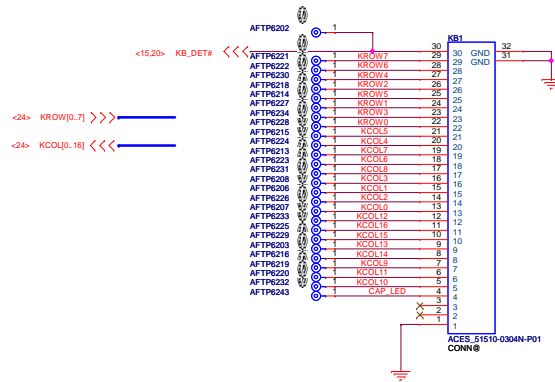
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						Size		Document Number		Rev	
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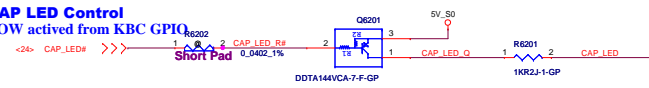
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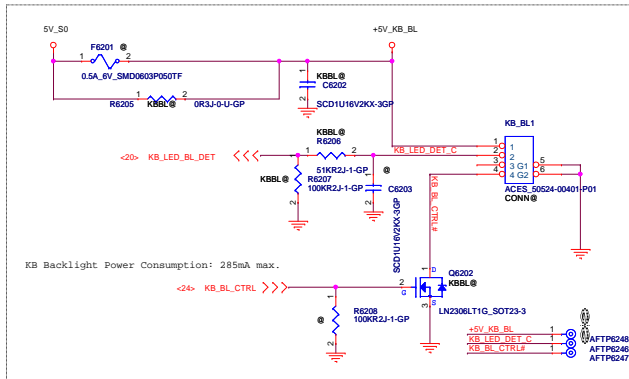
Internal Keyboard Connector (DVC40)



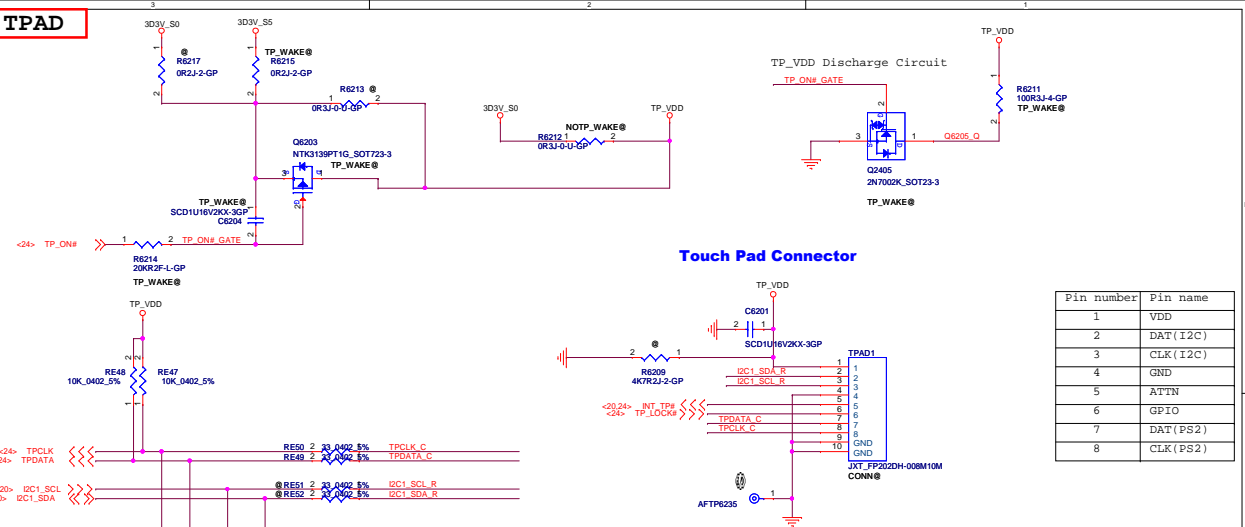
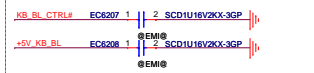
CAP LED Control
LOW activated from KBC GPIO



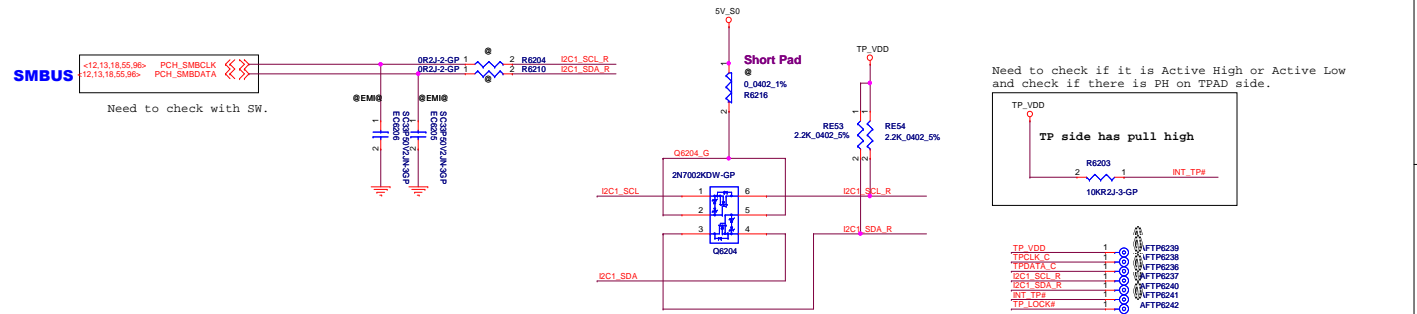
Keyboard Backlight (Reserved)



For EMI Reserved



RN6203 and PTP schematic are BOM option for verify I2C leakage issue.



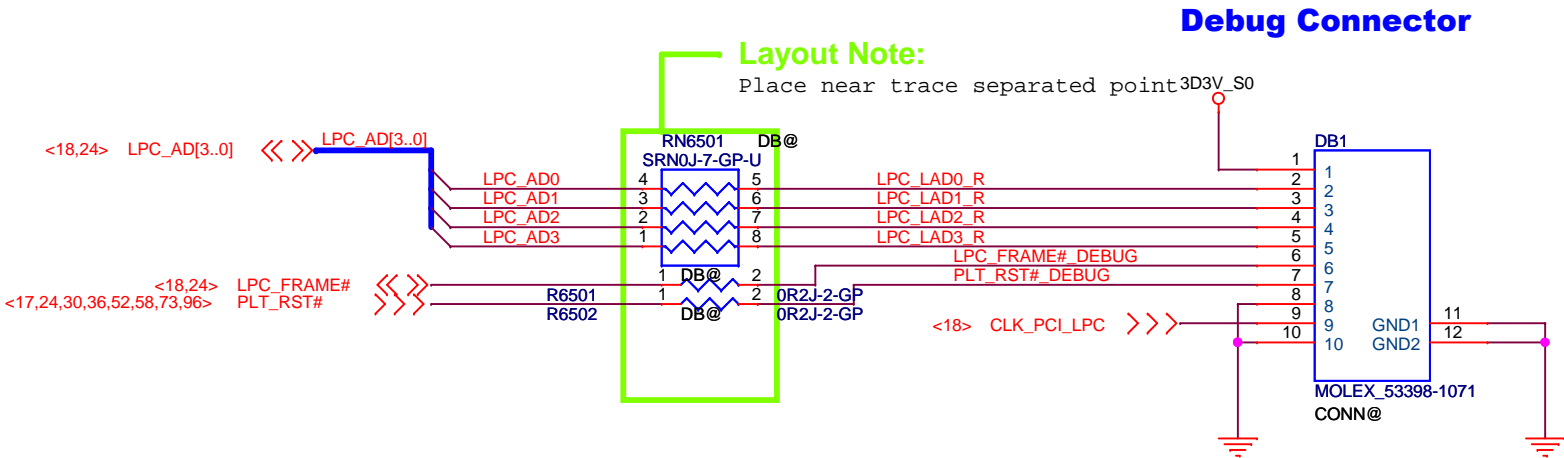
Main Func = Hall Sensor

Move to Power Button Board

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				Document Number		LA-B483P			
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Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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						Size		Document Number		Rev	
								<i>LA-B483P</i>		A00	
						Date:		Wednesday, January 21, 2015		Sheet 66 of 102	

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Main Func = dGPU

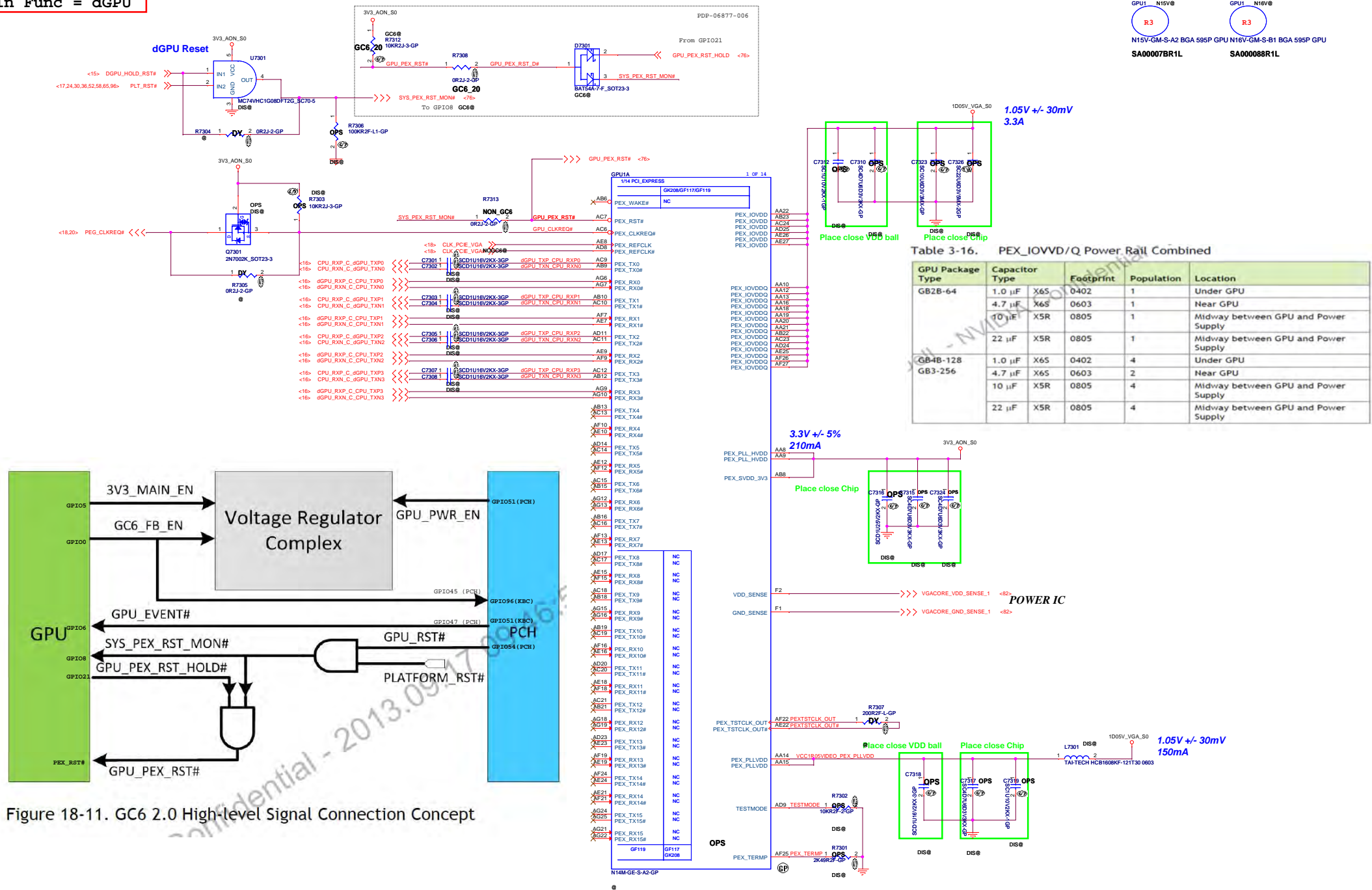
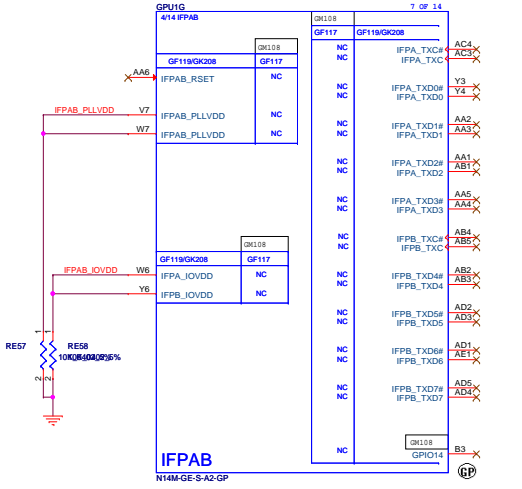


Figure 18-11. GC6 2.0 High-level Signal Connection Concept

N15V-GM-S-A2: JG0YH
N15S-GT is PXP79

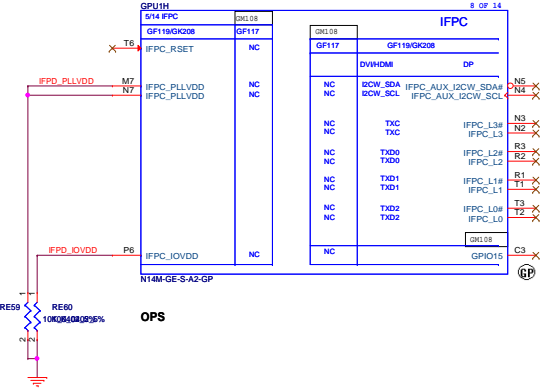
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LVDS Interface

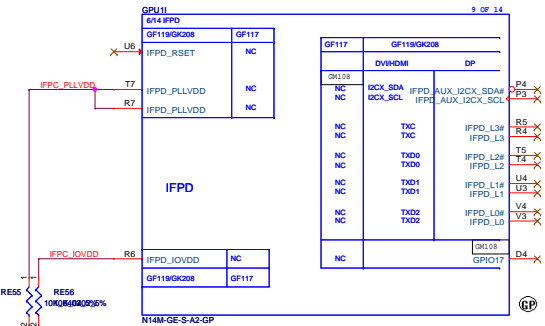


OPS

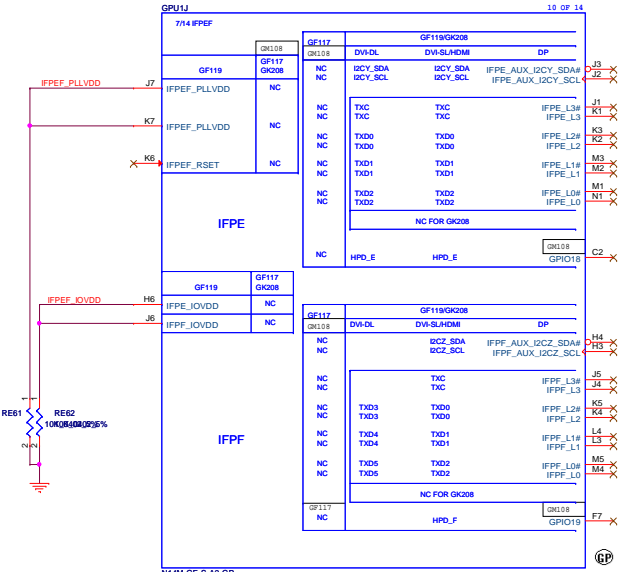
HDMI Interface



OPS



OPS



OPS

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU
GB4B-128 DDR3	0.1µF	X7R 0402	4	Under GPU
	1µF	X7R 0603	4	Under GPU
	4.7µF	X6S 0603	4	Under GPU
	10µF	X5R 0805	2	Near GPU

Notes:
1. The decoupling in this table applies to both single rank and dual rank designs.
2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

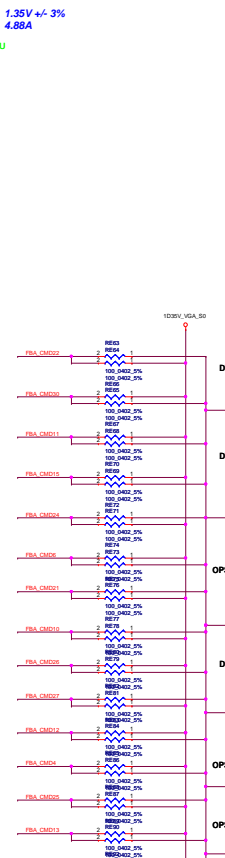
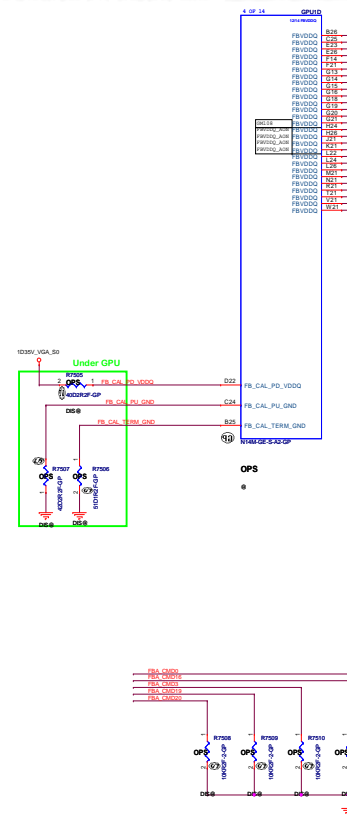
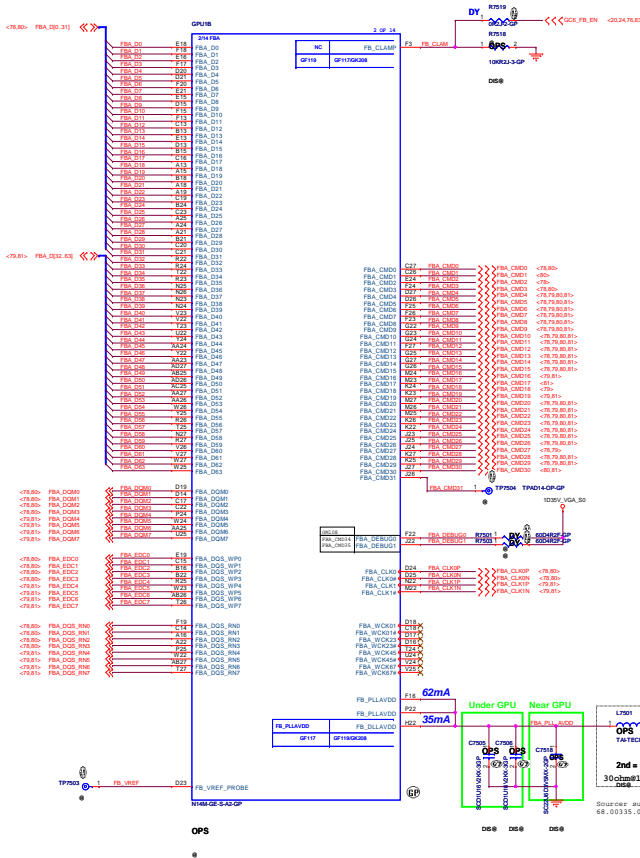


Table 6-4. Mode E Command Mapping

N15x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1	C51*		C51*	
FBx_CMD2	C50*		C50*	
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	BA5*	BA5*	BA5*	BA5*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16	ODT		ODT	
FBx_CMD17	C51*		C51*	
FBx_CMD18	C50*		C50*	
FBx_CMD19	CKE		CKE	
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33*				

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU

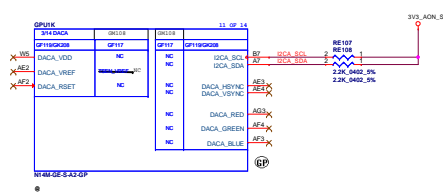
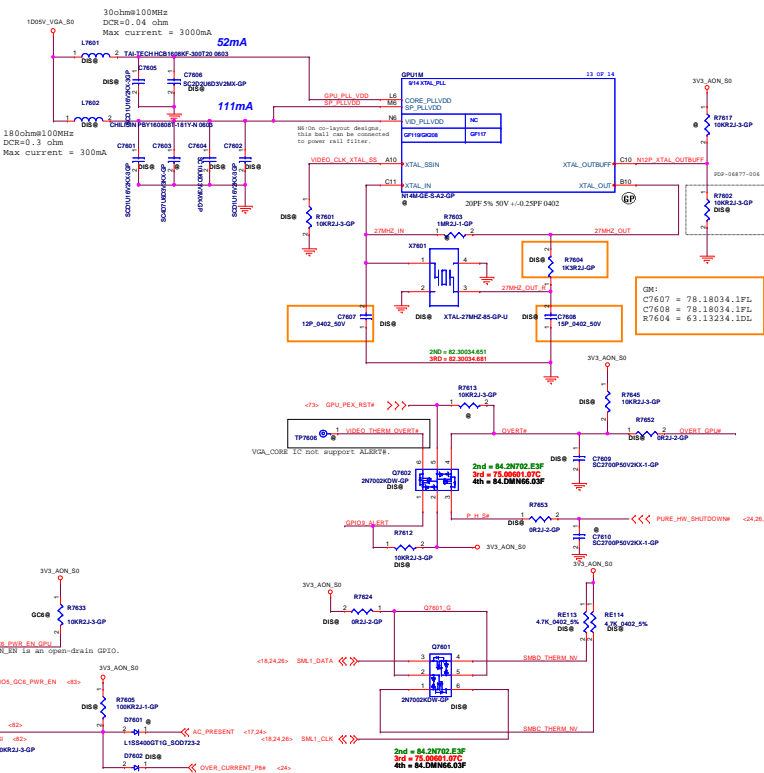
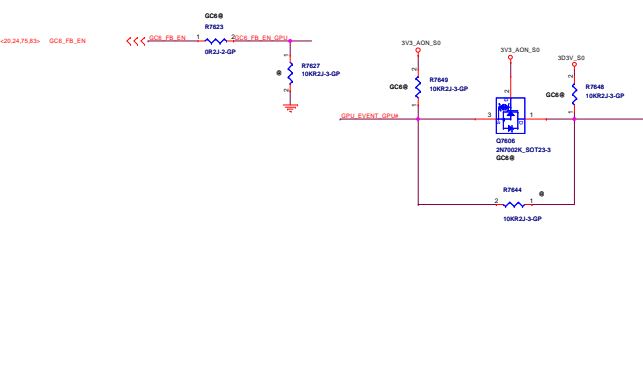
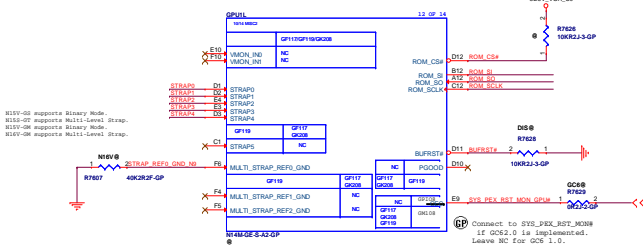
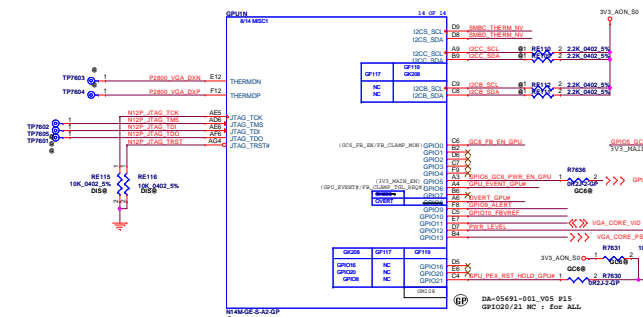


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 μ F	X7R D402	1	Under GPU
		22 μ F	XSR D805	1	Near GPU
		Bead Type	30 Ω (ESR=0.05 Ω)	D402	1
			D402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD + VID_PLLVDD	0.1 μ F	X7R D402	1 per ball	Under GPU
GB4B-128		4.7 μ F	XSR D603	1	Near GPU
GB3-256		2.2 μ F	XSR D805	1	Near GPU
		Bead Type	180 Ω (ESR=0.2 Ω)	D603	1
			D603	1	Near GPU



(RVL-06891-001)N15V-GT-S DDR3L Recommended Memories

Memory	GPU	Strap	Memory
128Mx16 DDR3L	Hynix	0x9	H5TC2G63PFR-11C
	Micron	0xA	MT41J128M16JT-093G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L (4 pcs VRAM)	Hynix	0x3	H5TC4G63AFR-11C
	Samsung	0x5	K4W4G1646D-BC1A
256Mx16 DDR3L (8 pcs VRAM)	Hynix	0xC	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0xE	K4W4G1646D-BC1A

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 k Ω	1000	0000
10.8 k Ω	1001	0001
15.0 k Ω	1010	0010
20.0 k Ω	1011	0011
24.9 k Ω	1100	0100
30.1 k Ω	1101	0101
34.9 k Ω	1110	0110
45.3 k Ω	1111	0111

Multi Strap-RAK[0:3:0]

R7640,R7641,R7642 for N155-GT 4 pcs VRAM

R7619,R7638,R639 for N155-GT 8 pcs VRAM

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

S0R4_EXPOSED=0000

Straps

(DB-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHIDOR	10k Ω	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See note below
STRAP1	RAM_CFG[1]	10k Ω	See note below
STRAP2	RAM_CFG[2]	10k Ω	See note below
STRAP3	RAM_CFG[3]	10k Ω	See note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

(RVL-06891-001)N15V-GM-S DDR3L Recommended Memories

Memory	GPU	Strap	Memory	STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63PFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

(DB-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H155-GV	PCI_DEVID[4]	SUB_VEHIDOR	PCI_DEVID[5]	PEX_PLL_EH_TERM
	H155-GM-GT	SOR1_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM GB2-64	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
	H155-GM	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	H155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	H155-GM-GT	DEVID_SEL	PCIE_CFG		
STRAP0	H155-GV	USER[3]	USER[2]	USER[1]	USER[0]
	H155-GM-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50k pull-up)			
STRAP1	H155-GV	3GIO_PADC[3]	3GIO_PADC[2]	3GIO_PADC[1]	3GIO_PADC[0]
	H155-GM-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	H155-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	H155-GM-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	H155-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	H155-GM-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	H155-GV	RESERVED	PCIE_SPEED_CHA	PCIE_MAX_SPEED	DP_PLL_VDD33V
	H155-GM-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 k Ω	1000	0000
10.8 k Ω	1001	0001
15.0 k Ω	1010	0010
20.0 k Ω	1011	0011
24.9 k Ω	1100	0100
30.1 k Ω	1101	0101
34.9 k Ω	1110	0110
45.3 k Ω	1111	0111

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 k Ω	1000	0000
10.8 k Ω	1001	0001
15.0 k Ω	1010	0010
20.0 k Ω	1011	0011
24.9 k Ω	1100	0100
30.1 k Ω	1101	0101
34.9 k Ω	1110	0110
45.3 k Ω	1111	0111

Table 15-2. Resistance Mapping to Hex Values

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Table 15-2. Resistance Mapping to Hex Values

Table 15-2. Resistance Mapping to Hex Values

Table 15-2. Resistance Mapping to Hex Values

Table 15-2. Resistance Mapping to Hex Values

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU
	1 μ F	X6S	0402	4	4	Under GPU
	47 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU
	4.7 μ F	X5R	0805	5	5	Near GPU
	330 μ F	POS	7343	1	1	Near GPU ESR \leq 6 m Ω

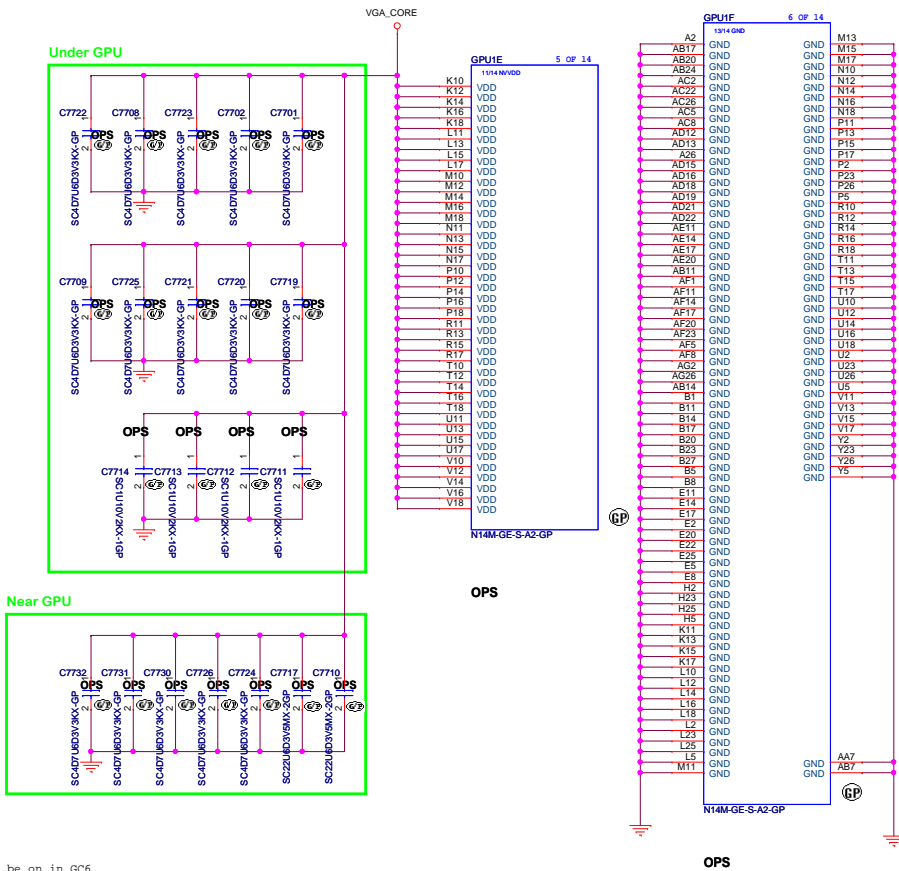
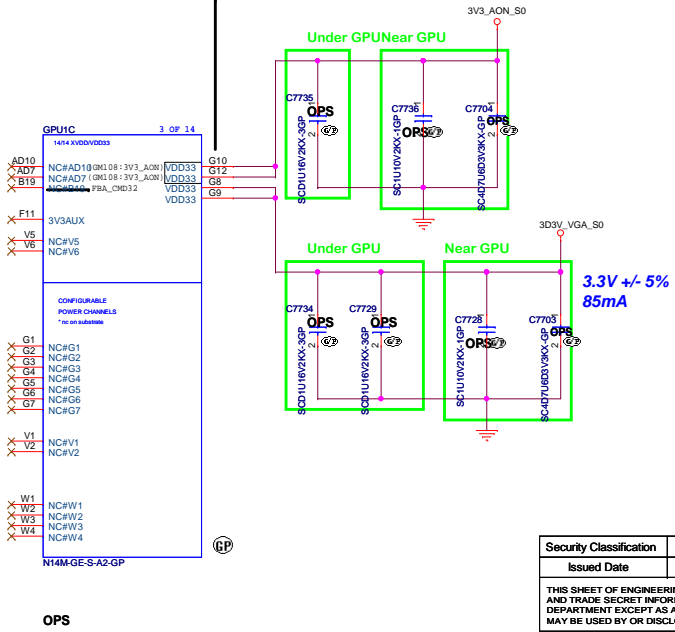


Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1 μ F	X6S	0402	2
GB4B-128		1 μ F	X5R	0603	1
GB3-256		4.7 μ F	X5R	0603	1
GB2B-64	3V3_AON	0.1 μ F	X6S	0402	1
GB4B-128		1 μ F	X5R	0603	1
GB3-256		4.7 μ F	X5R	0603	1

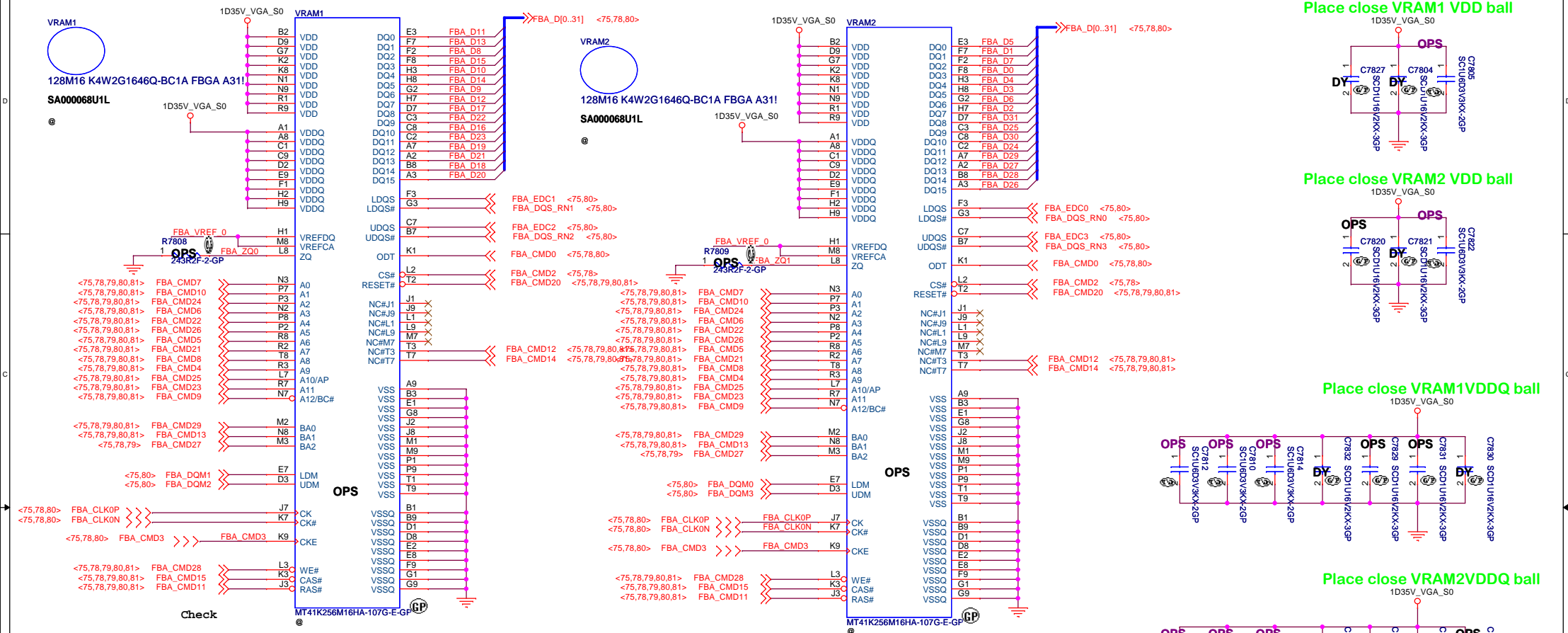
Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

G10, G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.

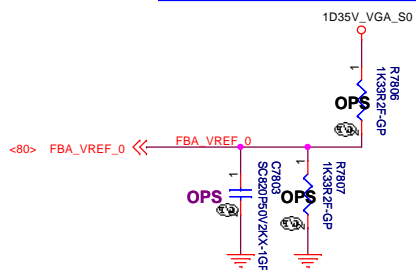


1GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	2Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 PCBGA595P	JG0YH	Hynix	H5TC2663FFR-11C	X1PRC	72.52663.N0U	1.35V	
		Samsung	K4W2G1646Q-BC1A	D0DP7	072.2G164.0A0U	1.35V	
		Micron	MT41K128M16JT-107G-K	HKKF2	72.41128.N0U	1.35V	
2GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 PCBGA595P	JG0YH	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41K256M16HA-107G-E	R5RH5	72.41K26.00U	1.35V	Build in EVT
4GB, Dual Rank, 8 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15S-GT-S-A2 GB2-64 PCBGA595	PXP79	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41J256M16HA-093G-E	PP8TP	072.41256.080U	1.35V	

Data Bits 31:0 RANK 0



Frame Buffer Patition A-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

FBCLK Termination place on VRAM side

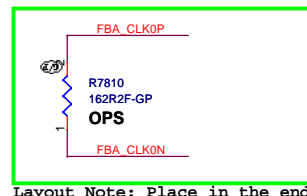
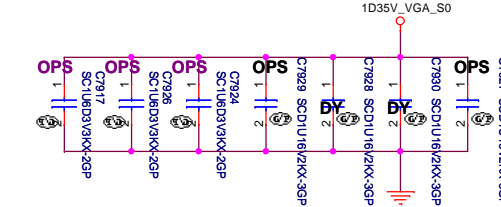
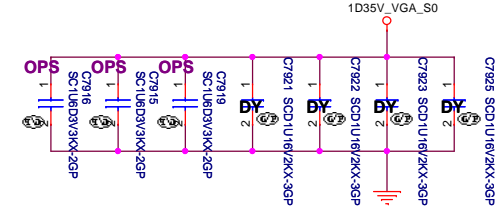
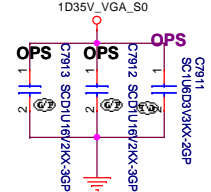
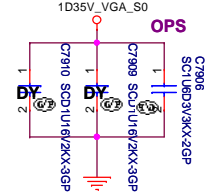
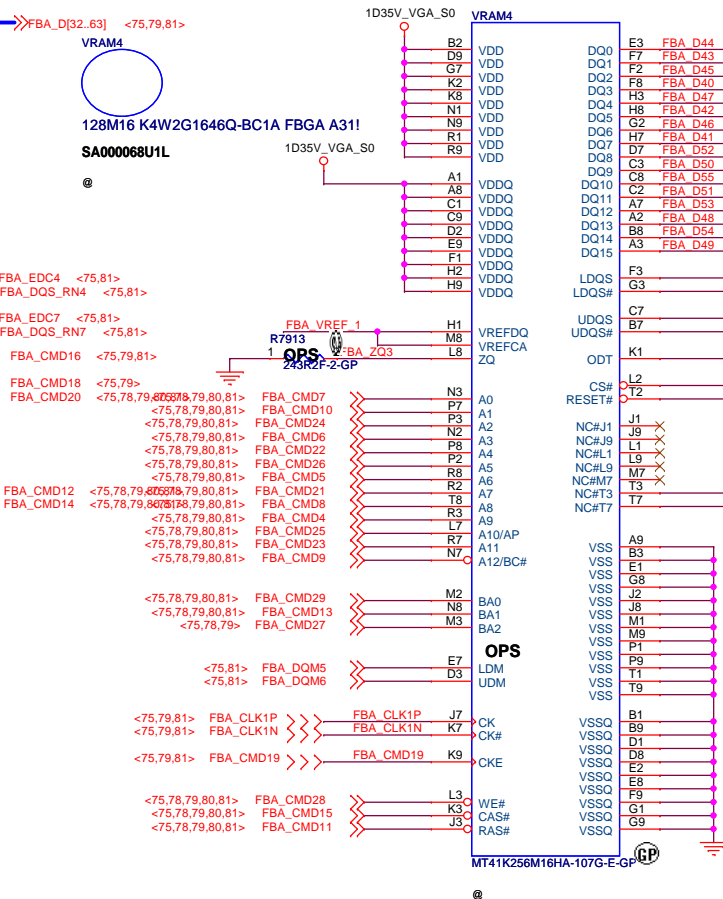


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

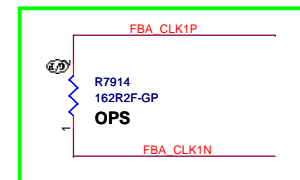
Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 μ F	X7R	0402	2		Under DRAM
1.0 μ F	X7R	0603	4		Under DRAM
10 μ F	X5R	0805	0		Close to DRAM

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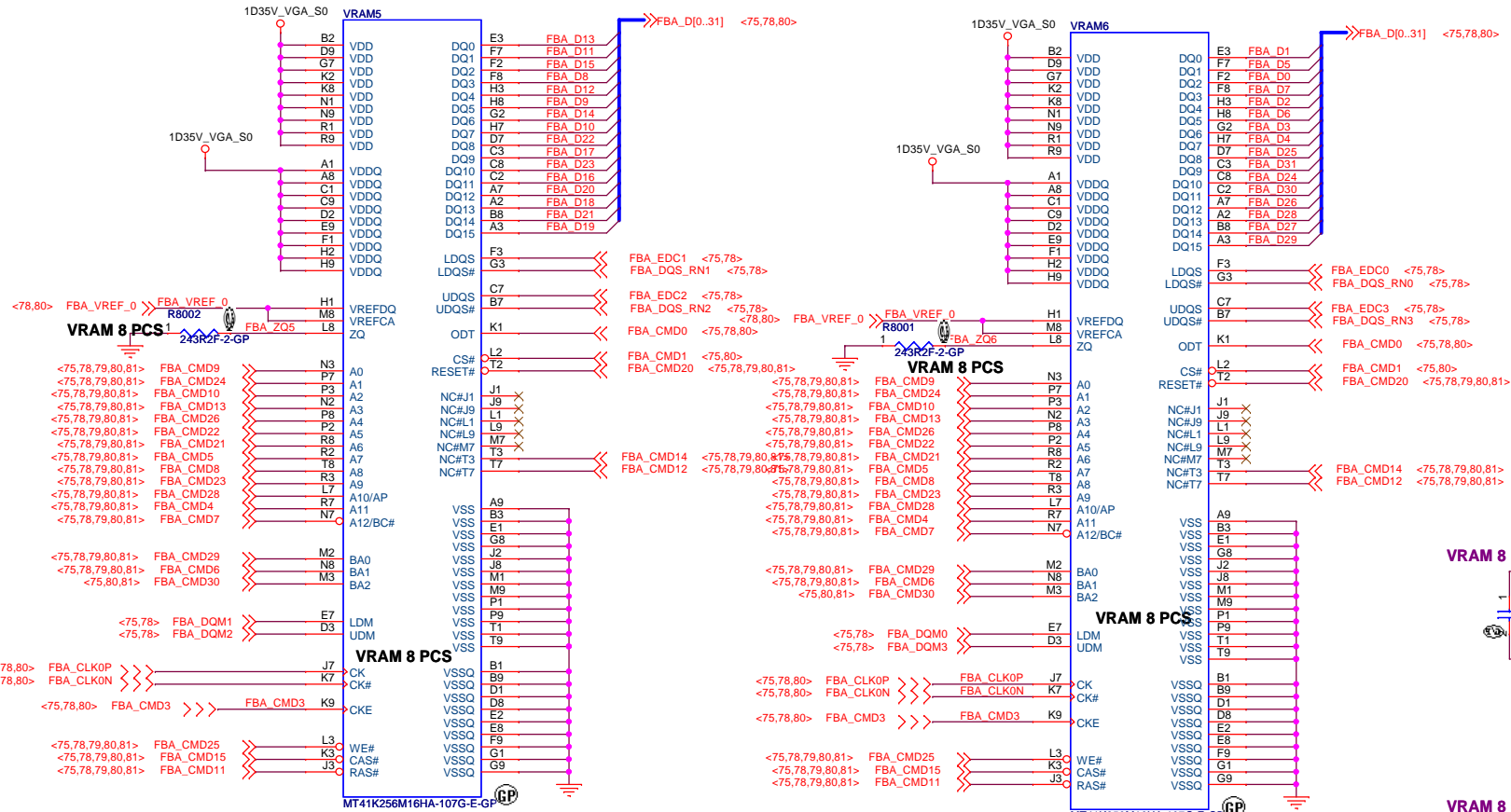


FBCLK Termination place on VRAM side

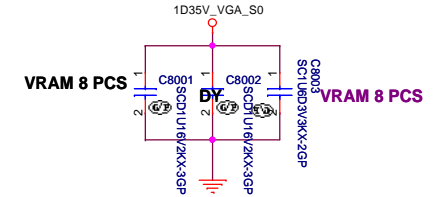


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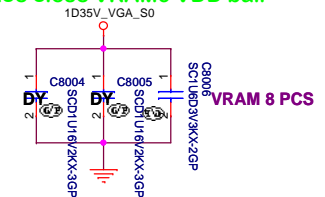
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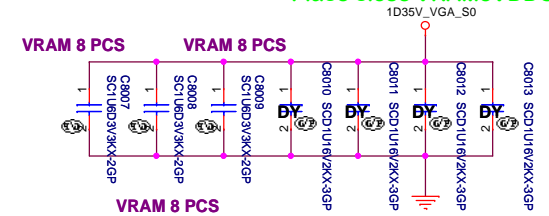
Place close VRAM5 VDD ball



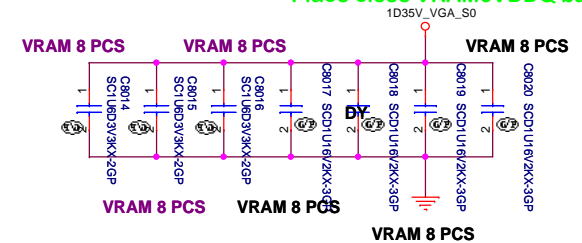
Place close VRAM6 VDD ball



Place close VRAM5VDDQ ball



Place close VRAM6VDDQ ball



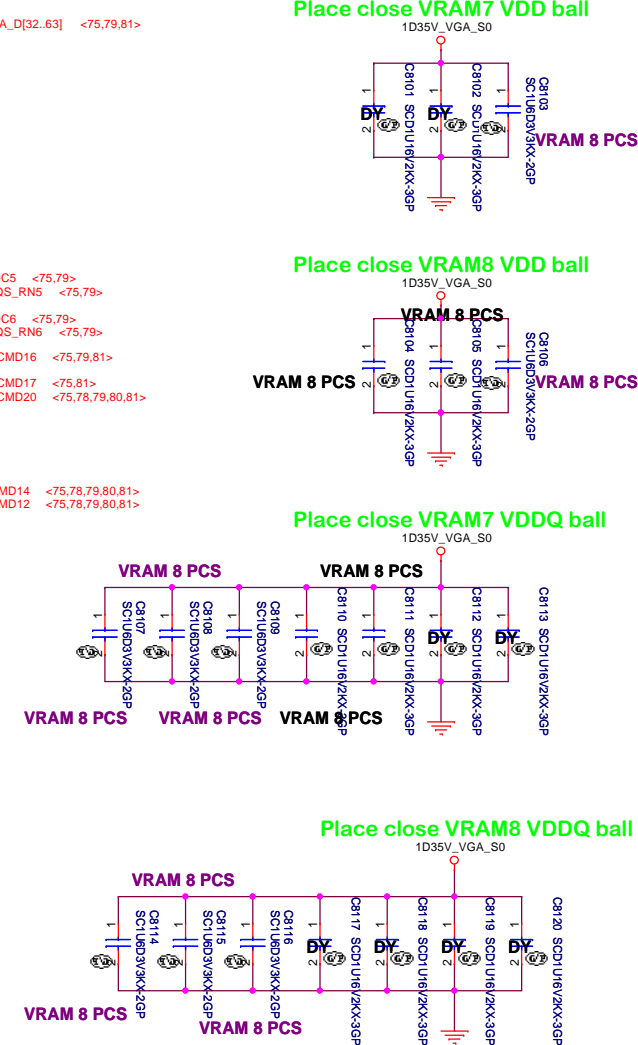
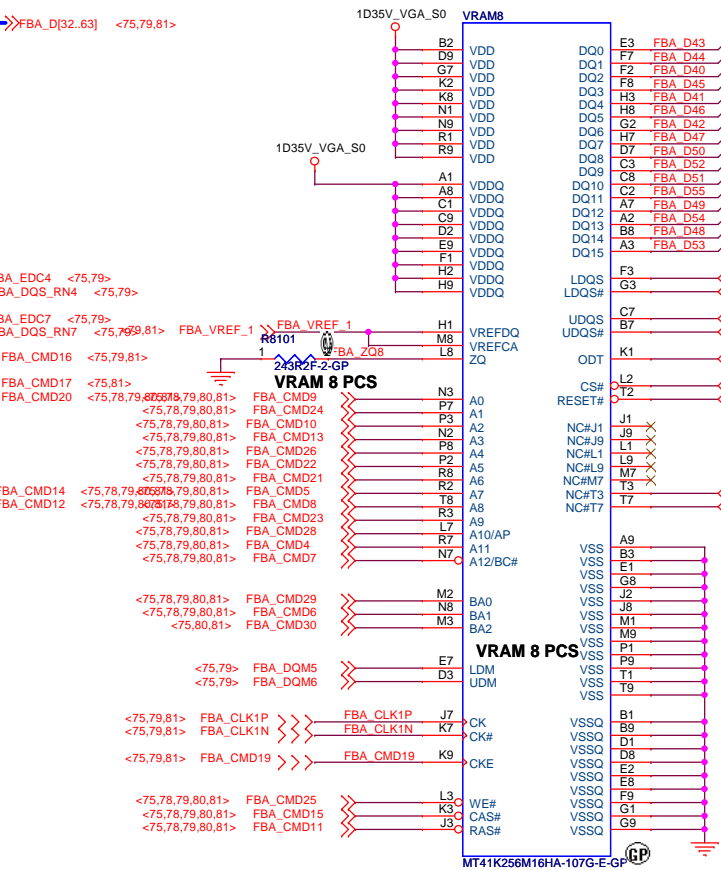
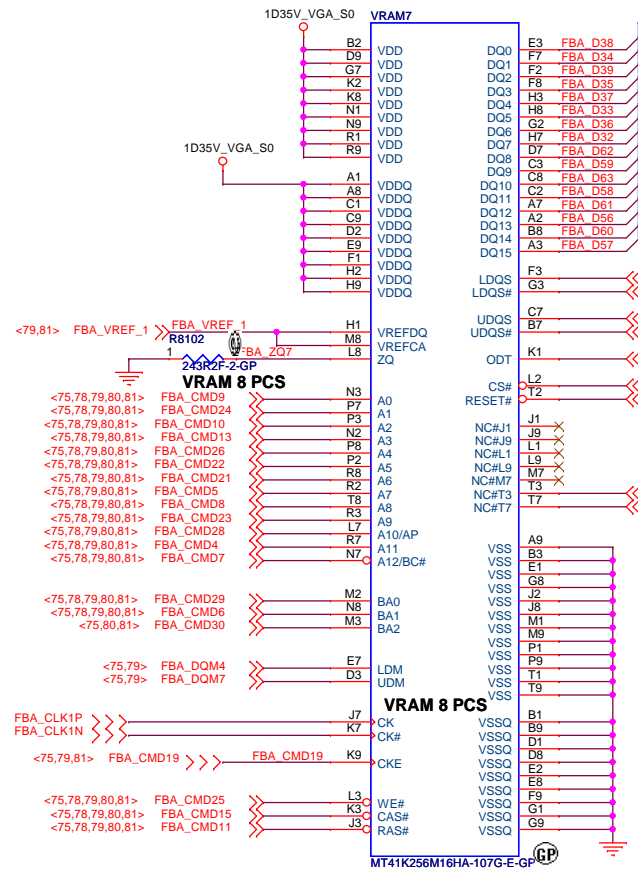
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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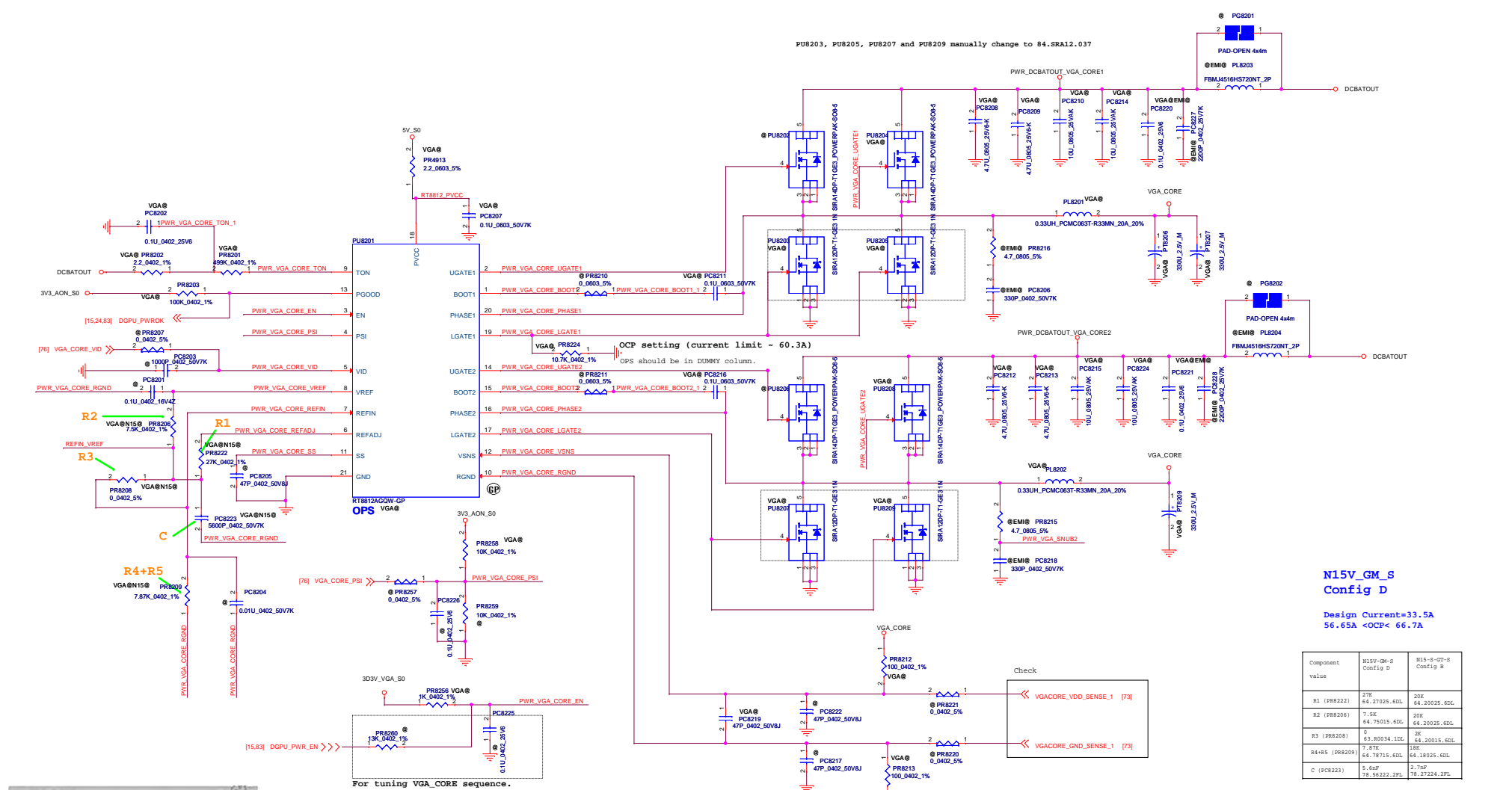
Main Func = dGPU

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PUB203, PUB205, PUB207 and PUB209 manually change to 84.SRA12.037



N15V_GM_S
Config D
Design Current=33.5A
56.65A <OCP< 66.7A

Component	N15V-GM-S Config D value	N15-G-07-S Config A
R1 (PR8222)	27K 64.27025, 60L	20K 64.20025, 60L
R2 (PR8206)	7.5K 64.75015, 60L	20K 64.20025, 60L
R3 (PR8208)	0 63.80034, 10L	2K 64.20015, 60L
R4+R5 (PR8209)	7.87K 64.78715, 60L	18K 64.18025, 60L
C (PC8223)	5.6nF 78.56222, 29F	2.7nF 78.27224, 29F

78.56222,29F:088 REASON: 50V is more popular, change to 78.56224,29F.

PWR-VID Specifications				
	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.6	0.6
Vmax	1.2	1.2	1.15	1.15
Vboot	0.875	0.875	0.9	1.028
Voltage Step Width	mV	4.25	25	42.5
Number of Voltage Levels N	level	56	30	30
PWM Frequency F _{sw}	MHz	1.125	0.876	0.876
PWM Minimum Pulse Width T _{min}	ns	9.26	74	74
V _D Transient Time T	-100	-100	-100	-100
Component Value				
R1 (R1)	KD	39	30	79
R2 (R1)	KD	39	30	7.5
R3 (R1)	KD	1.5	1	0
R4 (R1)	KD	30	18	24
R5 (R1)	KD	1.5	0	1.74
C	nF	1.5	2.7	5.6

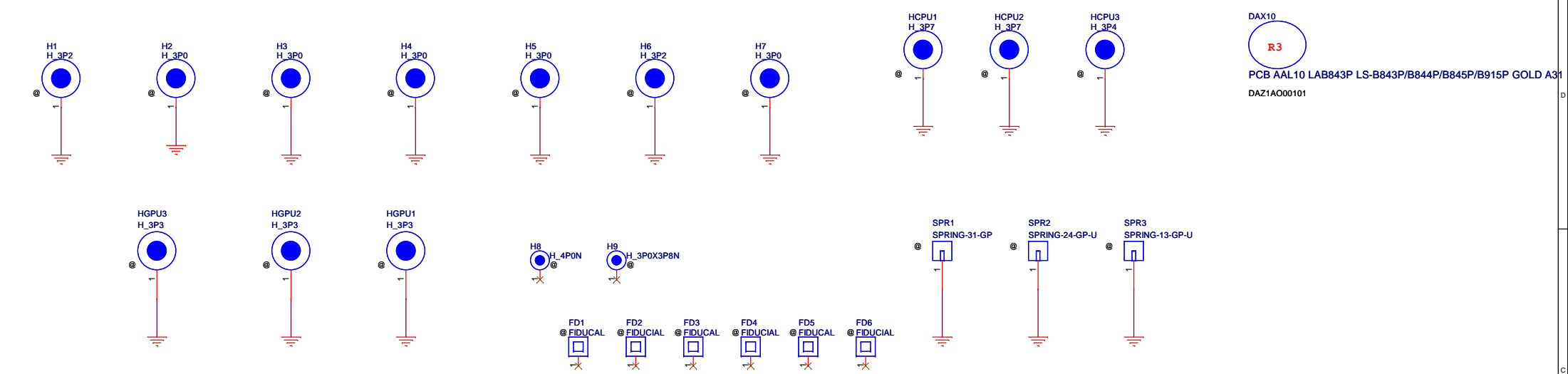


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

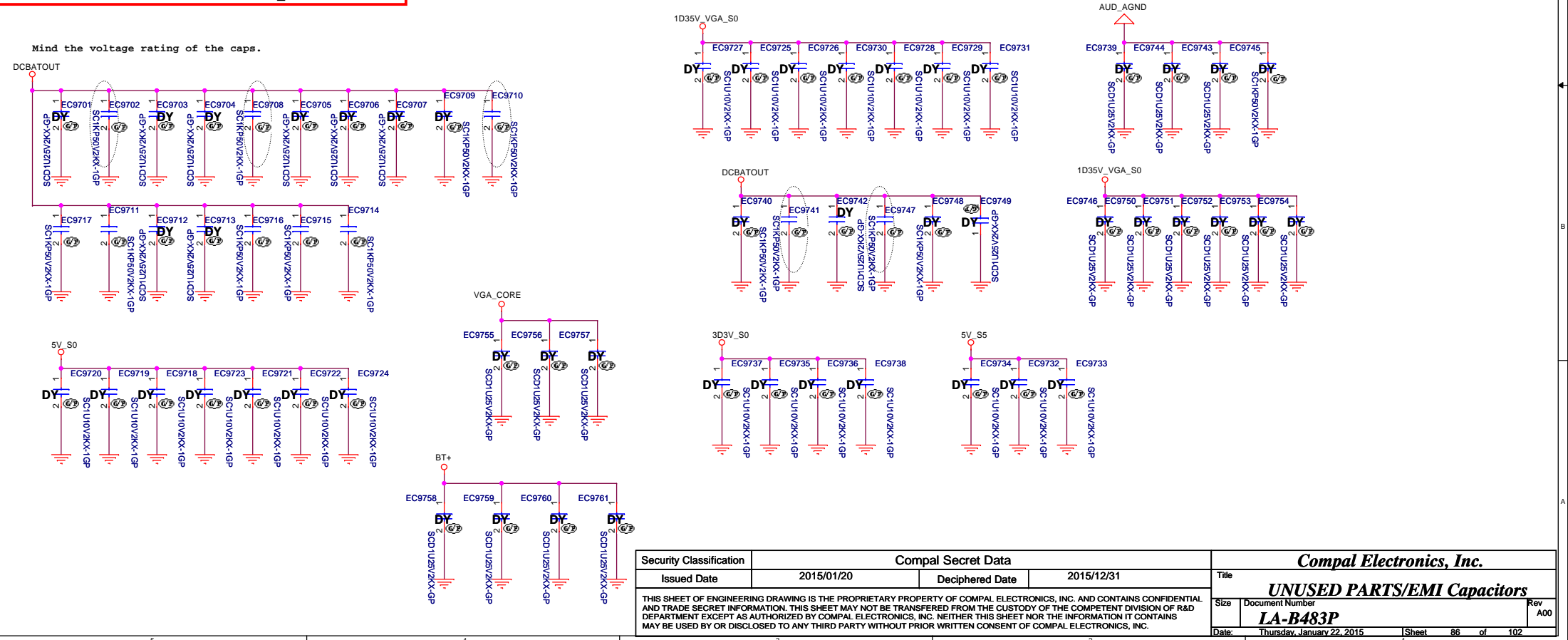
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Main Func = UnusedParts



Main Func = EMICapacitors



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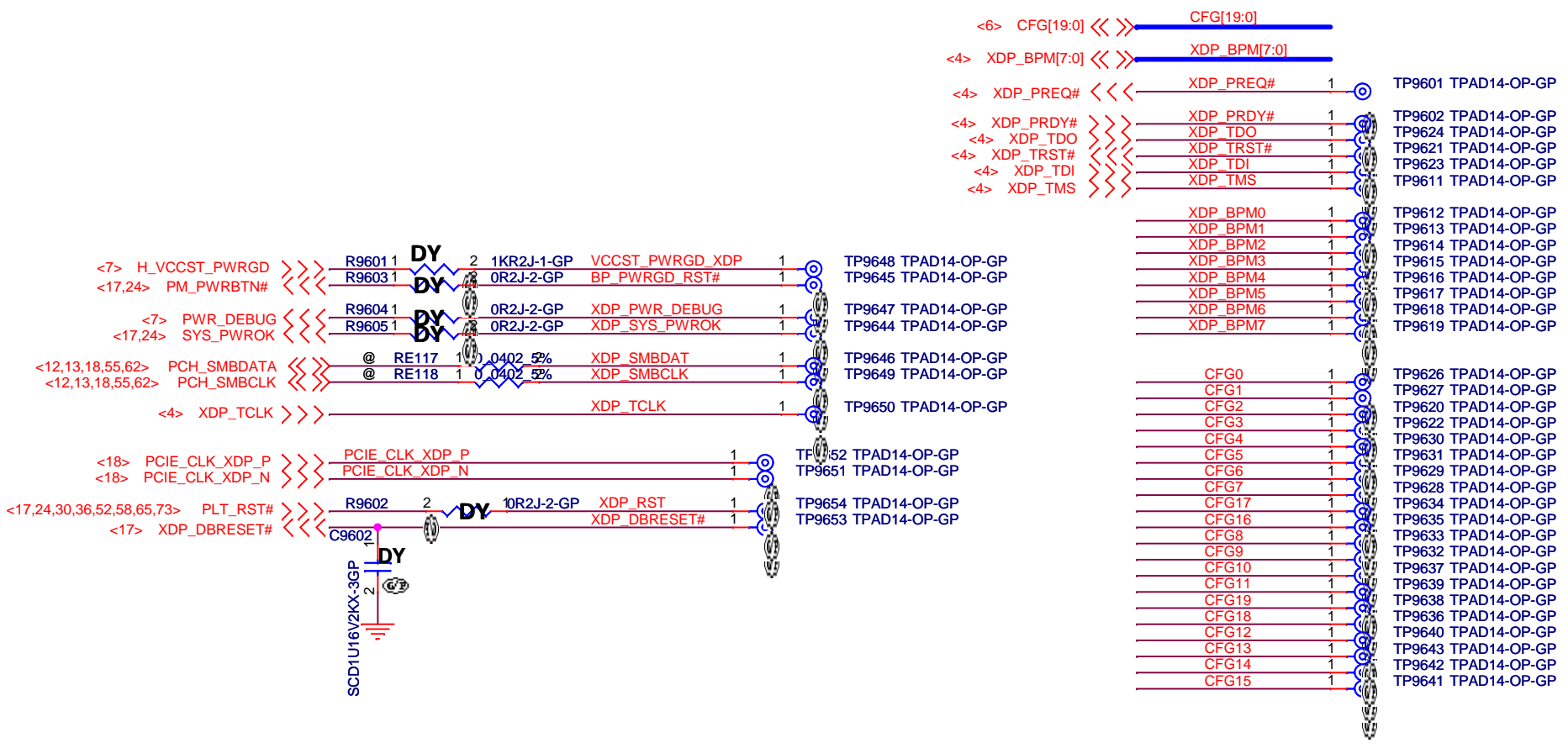
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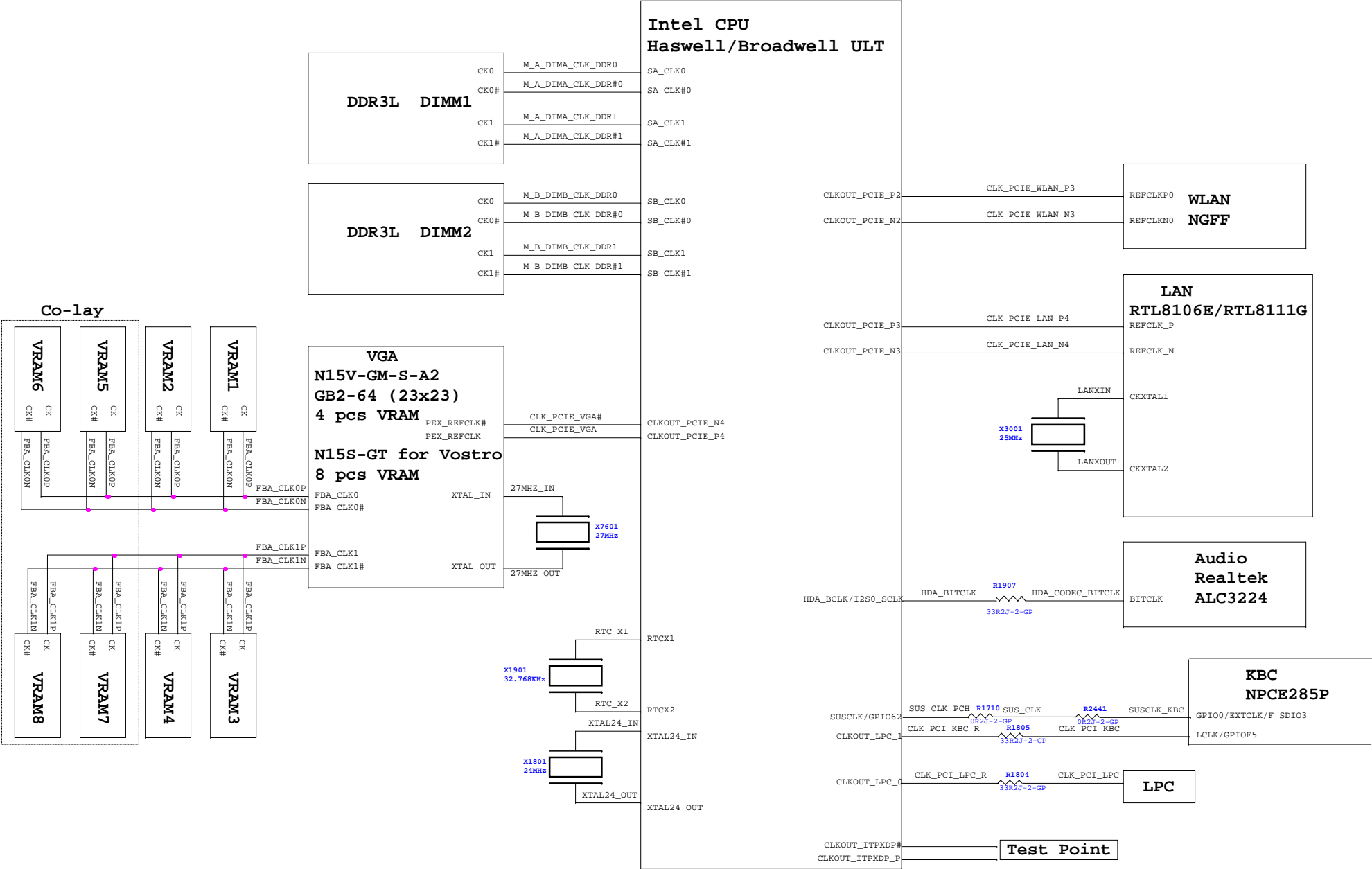
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CPU XDP



CLK Block Diagram

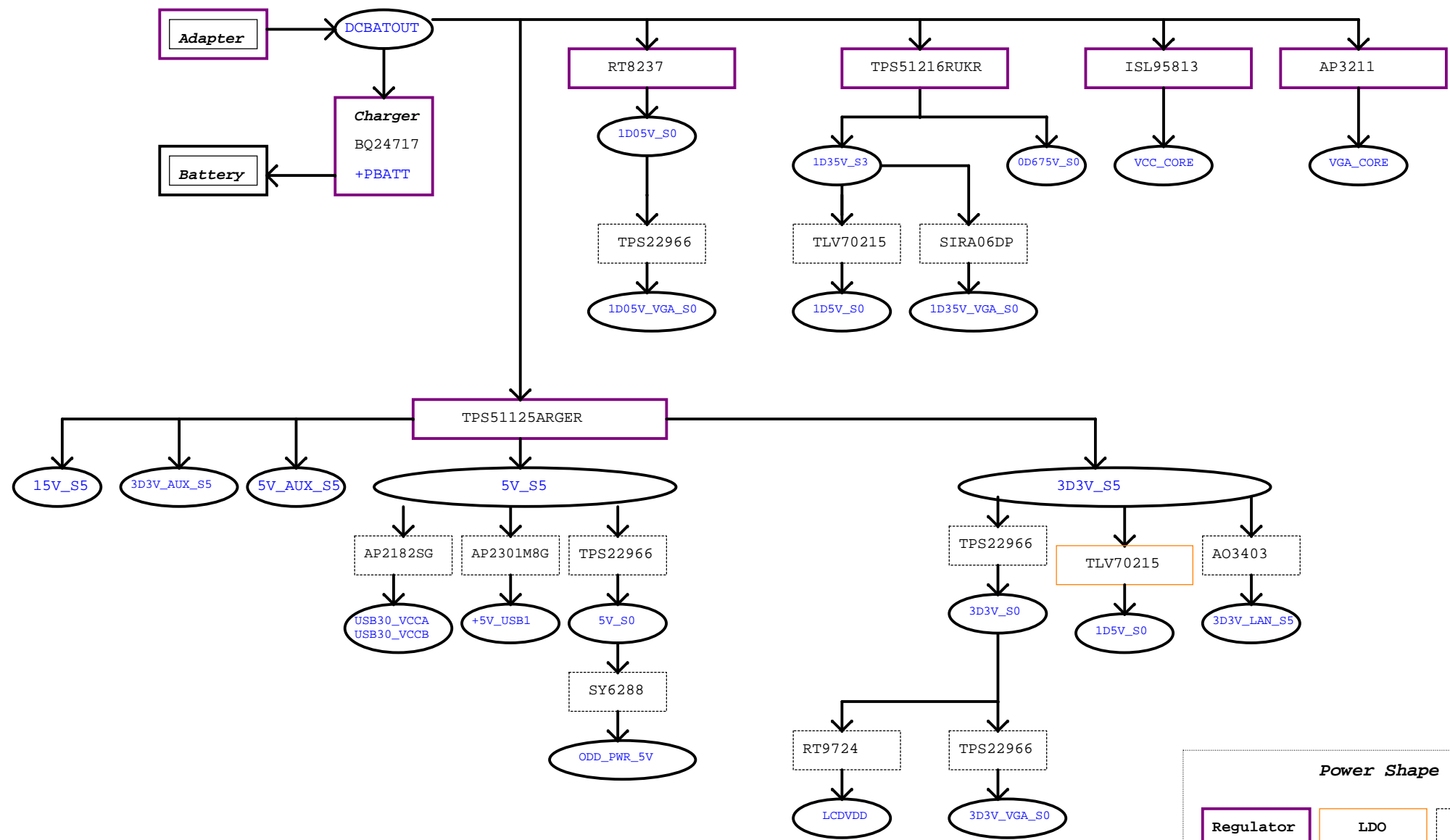


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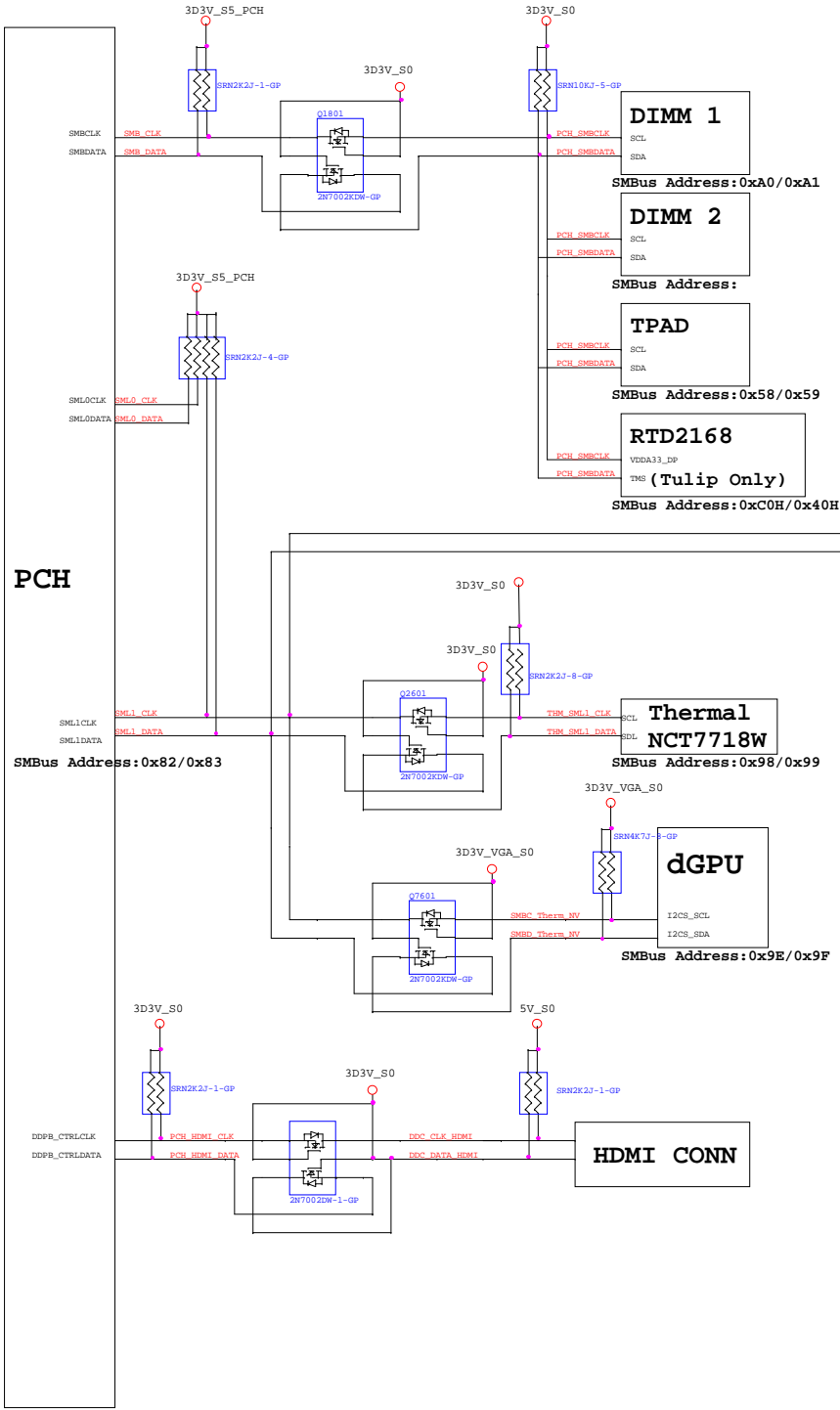
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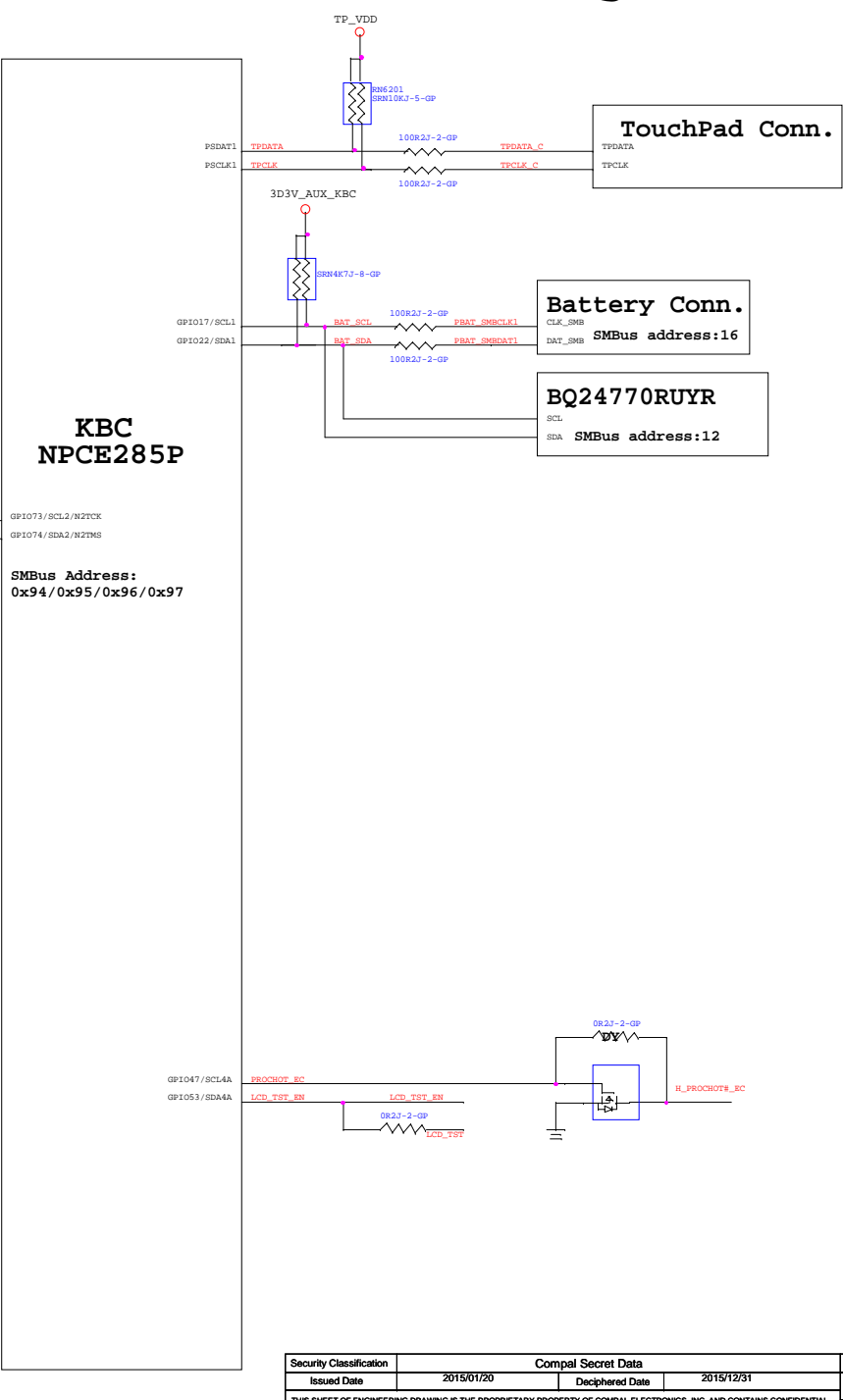
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PCH SMBus Block Diagram

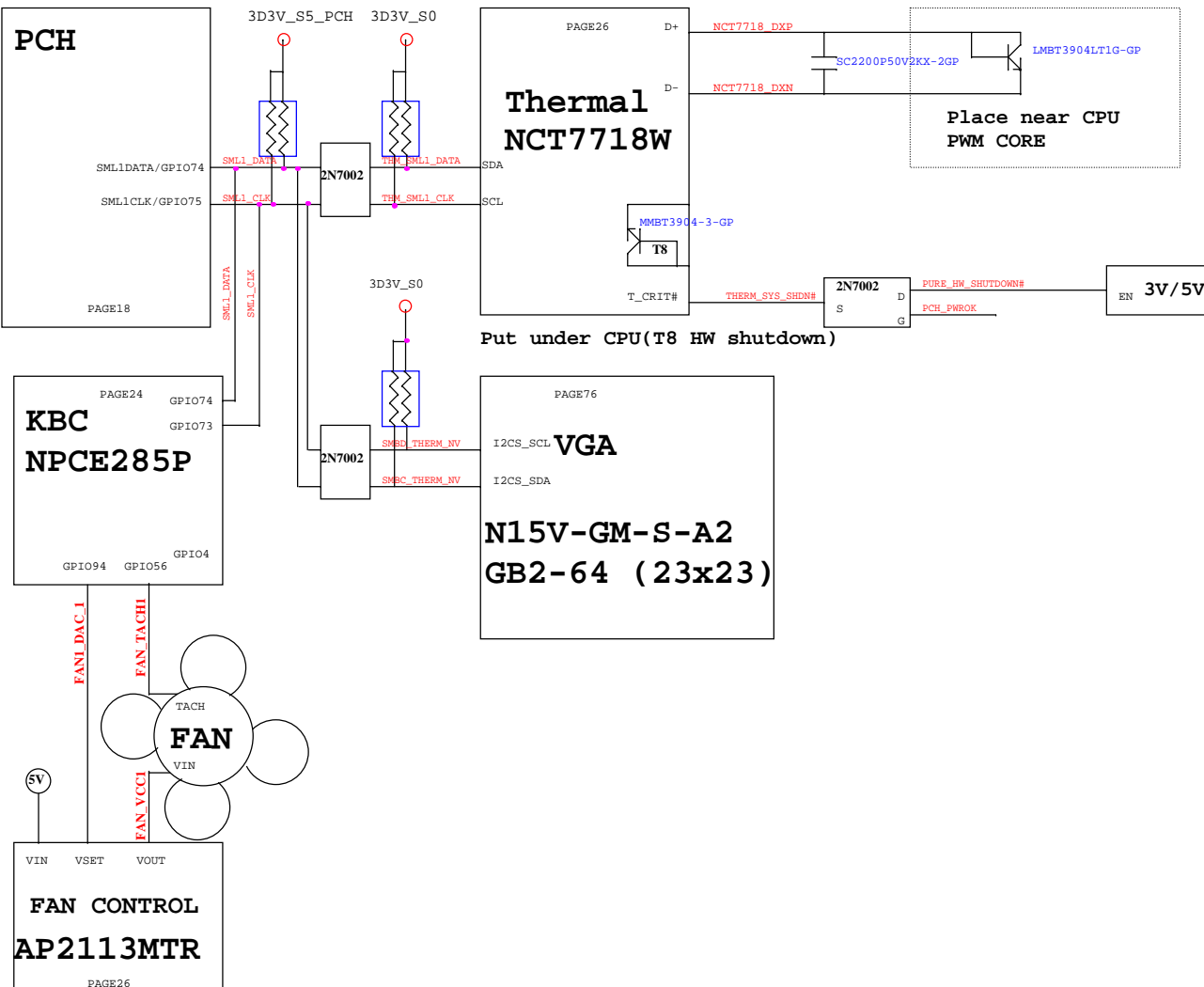


KBC SMBus Block Diagram

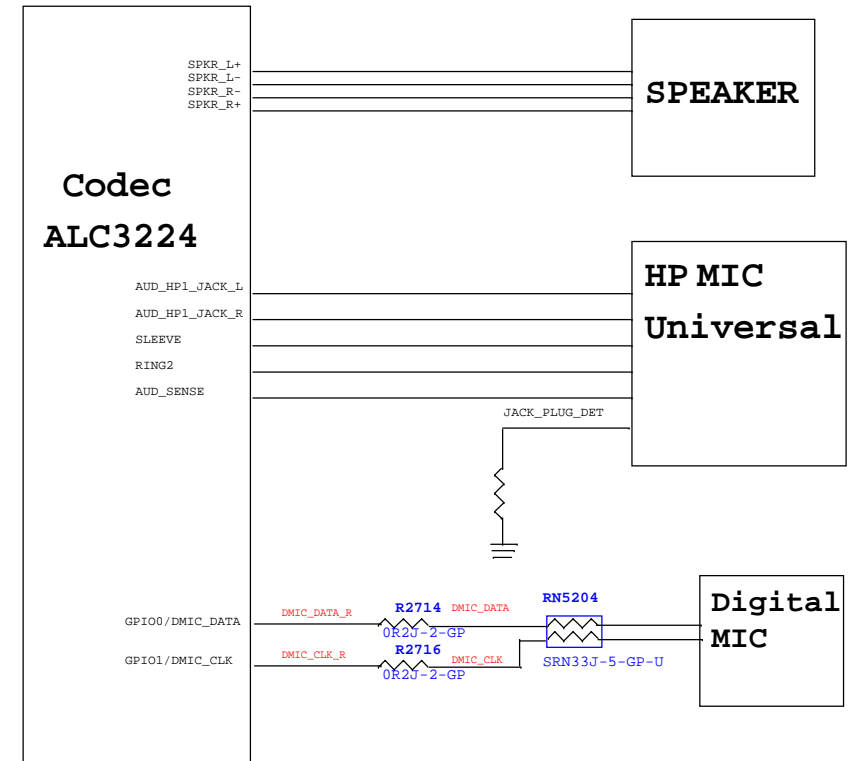


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Thermal Block Diagram



Audio Block Diagram



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